# 55 MHz to 15000 MHz Fractional-N PLL with Integrated VCO

Preliminary Technical Data

# ADF5610

## FEATURES

**RF bandwidth: 55 MHz to 15000 MHz**
**Maximum phase detector rate: 100 MHz**
**Industry leading Phase Noise**
**-115dBc/Hz Typical @ 100 kHz (7GHz)**
**114dBc/Hz Typical @ 100 kHz (10GHz)**
**-110dBc/Hz Max @ 100 kHz (15GHz)**
**RFOUT Power: +5dBm**
**Figure of Merit, Int / Frac (FOM): –229 / -226 dBc/Hz**
**24-bit step size, 3 Hz typical resolution**
**Exact frequency mode with 0 Hz frequency error**
**Fast frequency hopping**
**48-lead, 7 mm × 7 mm LFCSP package: 49 mm²**

## APPLICATIONS

**Cellular infrastructure**
**Microwave radios**
**WiMax, WiFi**
**Communications test equipment**
**CATV equipment**
**Military**
**Clocking**

## FUNCTIONAL BLOCK DIAGRAM

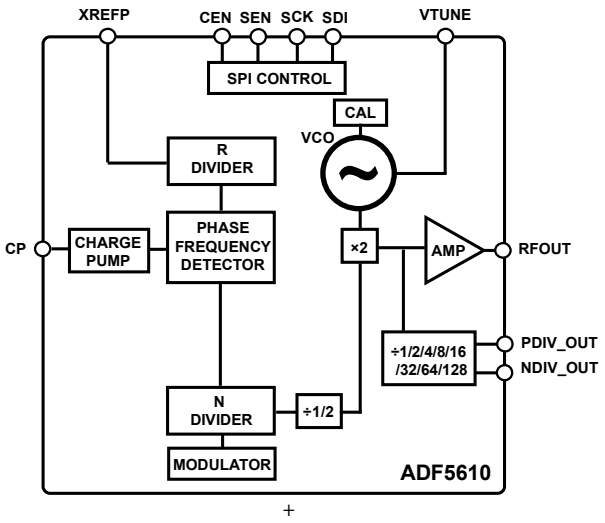


*Figure 1.*

## GENERAL DESCRIPTION

The ADF5610 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference source. The wideband microwave VCO design permits frequency operation from 7000 MHz to 15000 MHz at a single radio frequency (RF) output. A series of frequency dividers with a differential frequency output allows operation from 55 MHz to 15000 MHz. Analog and digital power supplies for the phase locked loop (PLL) circuitry range from 3.0 V to 3.6 V, and the voltage controlled oscillator (VCO) supplies are between 4.75 V to 5.25 V. The charge pump can be operated up to 3.6V for improved frequency band overlap and extended upper frequency range.

The ADF5610 has an integrated VCO with a fundamental frequency of 3500 MHz to 7000 MHz. These frequencies are internally doubled and routed to the RFOUT pin. An additional differential output allows the doubled VCO frequency to be divided by 1, 2, 4, 8, 16, 32, 64 and 128 allowing the user to generate RF output frequencies as low as 55 MHz. A simple 3-wire serial port interface (SPI) provides control of all on-chip registers. To conserve power, this divider block can be disabled when not needed through the SPI interface. Likewise, the output power for both the single ended and differential outputs are programmable via VCO registers settings. The ADF5610 also contains power-down modes for the VCO and PLL circuitry.

The integrated phase detector (PD) and delta-sigma (Δ-Σ) modulator, capable of operating at up to 100 MHz, permit wide loop bandwidths and fast frequency tuning with excellent spectral performance.

Industry leading phase noise and good spurious performance, across all frequencies, enable the ADF5610 to minimize blocker effects, and to improve receiver sensitivity and transmitter spectral purity. The low phase noise floor eliminates any contribution to modulator/mixer noise floor in transmitter applications.

The ADF5610 is a market leading PLL with integrated VCO. It features an innovative programmable performance technology that enables the ADF5610 to tailor current consumption and corresponding noise floor performance to individual applications by selecting either a low current consumption

**Rev. PrE** **Document Feedback**


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modes or a high performance mode for improved noise floor performance.

Additional features of the ADF5610 include 4dB of RFOUT gain control in 1 dB steps and approximately 6dB of control on the differential port in approximately 3dB steps. Finally the Δ-Σ modulator with exact frequency mode enables users to generate output frequencies with 0 Hz frequency error.

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# SPECIFICATIONS

$AV_{DD}$ = $DV_{DD}$ = 3.3 V ± 5%, VDDLS , VPPCP, RVDD, VDDPD, VCCPS, VCCHF = 3.3V ± 5%,

VDD1, VDD2, VDD3 = 3.3V±10%, VCCVCO = 5.0V ± 5%, GND = 0 V,

Minimum and maximum specified across the temperature range of −40°C to +85°C.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **RF OUTPUT CHARACTERISTICS** | | | | | |
| RFOUT Frequency | | 7000 | | 15000 | MHz |
| VCO Frequency at PLL Input | | 3500 | | 7000 | MHz |
| Frequency Range PDIV / NDIV | | 55 | | 15000 | MHz |
| **OUTPUT POWER** | | | | | |
| RFOUT Power | Across all frequencies, high performance mode (VCO_REG 0x01[11:9] = 0x3), Maximum gain setting (VCO_REG 0x01[8:7] = 0x3) | 0 | 5 | 10 | |
| RFOUT Power Control Range | 1 dB steps | | 4 | | dB |
| RFOUT Power Variation vs Temperature | | | ±2 | | dBm |
| RFOUT Power Variation vs Frequency | | | ±3 | | dBm |
| PDIV / NDIV Power | Maximum gain setting (VCO_REG 0x01[13:12] = 0x3), single-ended | -2 | 0 | 2 | dBm |
| | Divide-by-2 to divide-by-128 | | 2 | | dBm |
| PDIV / NDIV Control Range | 3 settings, bypass mode (divide-by-1) | | 6 | | dB |
| **HARMONICS (RFOUT)** | | | | | |
| ½ Harmonic | (3500MHz – 7500MHz) | | -20 | | dBc |
| 1.5 Harmonic | | | -30 | | dBc |
| 2nd Harmonic | | | -30 | | dBc |
| 2.5 Harmonic | | | -35 | | dBc |
| 3rd Harmonic | | | -30 | | dBc |
| **VCO OUTPUT DIVIDER** | | | | | |
| VCO RF Divider Range | 1, 2, 4, 6, 8, … 128 | 1 | | 128 | |
| **HARMONICS (PDIV / NDIV )** | | | | | |
| Fundamental Feedthrough Outputs (N = 1) | Measured single-ended | | -20 | | dBc |
| Push-Push Feedthrough (N=2) | Measured single-ended | | -24 | | dBc |
| **PLL RF DIVIDER CHARACTERISTICS** | | | | | |
| 19-Bit N-Divider Range (Integer) | Maximum = $2^{19}$ – 1 | 16 | | 524,287 | |
| 19-Bit N-Divider Range (Fractional) | Fractional nominal divide ratio varies (±4) dynamically maximum | 20 | | 524,283 | |
| **REFERENCE INPUT CHARACTERISTICS** | | | | | |
| Maximum XREFP Input Frequency | | | | 350 | MHz |
| XREFP Input Level | AC-coupled[1] | –6 | | +12 | dBm |
| XREFP Input Capacitance | | | | 5 | pF |
| 14-Bit R-Divider Range | | 1 | | 16,383 | |
| **PHASE DETECTOR (PD)[2]** | | | | | |
| PD Frequency Fractional Mode[3] | | DC | | 100 | MHz |
| PD Frequency Integer Mode | | DC | | 100 | MHz |
| **CHARGE PUMP** | | | | | |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Current | | 0.02 | | 2.54 | mA |
| Charge Pump Gain Step Size | | | 20 | | µA |
| **LOGIC INPUTS** | 1.8 V and 3.3 V modes | | | | |
| Input Voltage | | | | | |
| Low ($V_{IL}$) | | | | 0.75 | V |
| High ($V_{IH}$) | | 1.15 | | | V |
| SCK Clock Frequency Rate | | | 6 | 50 | MHz |
| | | | | | |
| **LD/SDO LOGIC OUTPUT** | | | | | |
| Output High Voltage | | | | | |
| | CMOS 3.3 V mode (Register 0x0F[9:8] = 00b) | $V_{DD}$ – 0.2 | | $V_{DD}$ | V |
| | Open-drain mode (Register 0x0F[9:8] = 01b)[4] | | | 3.3 | V |
| Low ($V_{OL}$) | CMOS mode (Register 0x0F[9:8] = 00b) | | | 0.1 | V |
| | Open-drain mode (Register 0x0F[9:8] = 01b)[5] | | 0.4 | | |
| SCK Clock Frequency Rate | CMOS mode (Register0x0F[9:8] = 00b)[6] | | 6 | 50 | MHz |
| | Open-drain mode (Register0x0F[9:8] = 01b)[7] | | 5 | 10 | MHz |
| Capacitive Load | CMOS mode (Register0x0F[9:8] = 00b) | | 10 | 20 | pF |
| | Open-drain mode (Register0x0F[9:8] = 01b)[8] | | | 10 | pF |
| Load Current | CMOS mode (Register0x0F[9:8] = 00b)[9] | | | 3.6 | mA |
| | Open-drain mode (Register0x0F[9:8] = 01b)[10] | | | 7.2 | mA |
| Output Resistance When Driver Is Low ($R_{ON}$) | Open-drain mode (Register0x0F[9:8] = 01b) | | 100 | 200 | Ω |
| Pull-Up Resistor ($R_{UP}$) | Open-drain mode (Register0x0F[9:8] = 01b) | 500 | 1000 | | Ω |
| Rise Time | CMOS mode (Register0x0F[9:8] = 00b)[11] | | 0.5 + 0.3($C_{LOAD}$) | 7 | ns |
| Fall Time | CMOS mode (Register0x0F[9:8] = 00b)[11] | | 1.5 + 0.2($C_{LOAD}$) | 10 | ns |
| SCK to SDO Turnaround Time | CMOS mode (Register0x0F[9:8] = 00b)[11] | | 0.9 + 0.1($C_{LOAD}$) | 12 | ns |
| **POWER SUPPLY VOLTAGES** | | | | | |
| 3.3 V Supplies | AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD, VPPCP, VDDLS, VDD1, VDD2,VDD3 | 3.1 | 3.3 | 3.5 | V |
| 5.0 V Supplies | VCOVCC | 4.75 | 5.0 | 5.25 | |
| **POWER SUPPLY CURRENTS** | | | | | |
| AVDD | 3.3 V | | 1.6 | | mA |
| RVDD | 3.3 V | | 6 | | mA |
| VCCHF | 3.3 V | | 4 | | mA |
| VCCPS | 3.3 V | | 29.7 | | mA |
| VCCPD | 3.3 V | | 1.0 | | mA |
| DVDD | 3.3 V | | 11.9 | | mA |
| VPPCP[12] | 3.3 V | | 5.6 | | mA |
| VDDLS[12] | 3.3 V | | 0.6 | | mA |
| VDD1 | 3.3 V | | 3 | | mA |
| VDD2 | 3.3 V | | 1 | | mA |
| VDD3 | Divide-by-1 / Divide-by-128 | | 62 / 92 | | mA |
| VCOVCC | 5.0V | | 110 | | mA |
| **Power-Down** | | | | | |
| PLL[13] | Power Down via spi REG 0x01[0] = 0 and REG0x01[1] = 0 | | 100 | | uA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCOVCC[14] | Power Down using VCO_REG0x02[10] = 1 | | 13 | | mA |
| Divider[15] | Power Down using VCO_REG0x01[15] = 0 | | 1.5 | | mA |
| **POWER-ON RESET** | | | | | |
| Typical Reset Voltage on DVDD | | | 700 | | mV |
| Minimum DVDD Voltage for No Reset | | 1.5 | | | V |
| Power-On Reset Delay | | | 250 | | µs |
| **VCO CLOSED-LOOP PHASE NOISE** | | | | | |
| RFOUT at 10000 MHz, 100 kHz Offset | See Figure 8 | | –113 | | dBc/Hz |
| **VCO OPEN-LOOP PHASE NOISE** | | | | | |
| RFOUT at 7 GHz | | | | | |
| 10 kHz Offset | | | –92 | | dBc/Hz |
| 100 kHz Offset | | | –116 | | dBc/Hz |
| 1 MHz Offset | | | –136 | | dBc/Hz |
| 10 MHz Offset | | | –156 | | dBc/Hz |
| 100 MHz Offset | | | –165 | | dBc/Hz |
| RFOUT at 10 GHz | | | | | |
| 10 kHz Offset | | | –92 | | dBc/Hz |
| 100 kHz Offset | | | –114 | | dBc/Hz |
| 1 MHz Offset | | | –135 | | dBc/Hz |
| 10 MHz Offset | | | –155 | | dBc/Hz |
| 100 MHz Offset | | | –161 | | dBc/Hz |
| RFOUT at 11 GHz | | | | | |
| 10 kHz Offset | | | –89 | | dBc/Hz |
| 100 kHz Offset | | | –112 | | dBc/Hz |
| 1 MHz Offset | | | –132 | | dBc/Hz |
| 10 MHz Offset | | | –152 | | dBc/Hz |
| 100 MHz Offset | | | –161 | | dBc/Hz |
| RFOUT at 15 GHz | | | | | |
| 10 kHz Offset | | | -87 | | |
| 100 kHz Offset | | | -110 | | dBc/Hz |
| 1 MHz Offset | | | –131 | | dBc/Hz |
| 10 MHz Offset | | | –151 | | dBc/Hz |
| 100 MHz Offset | | | –158 | | dBc/Hz |
| **PLL** | | | | | |
| Phase Noise at 20 kHz Offset, 50 MHZ PFD Rate | Over process with 3.3 V power supply at 25°C, measured with >200 kHz loop bandwidth | | | | |
| Lock Time | Depends on loop filter bandwidth, PFD rate, and definition of lock (to within ±Hz or ±degrees of settling) | | 500 | | µs |
| Frequency Resolution | Depends on PFD rate and VCO output divider setting | | | | |
| Fundamental Mode | 3.5 GHz to 7.5 GHz output; at typical phase detector frequency ($f_{PD}$) of 50 MHz, typical resolution = 3 Hz | | $f_{PD}/2^{24}$ | | Hz |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Divider Mode | <3.5 GHz output, resolution depends on VCO output divider setting | | $f_{PD}/(2^{24} \times$ output divider) | | Hz |
| Reference Spurs | | | −85 | | dBc/Hz |
| **FIGURE OF MERIT (FOM)** | Normalized to 1 Hz | | | | |
| Floor Integer Mode | | | −229 | | dBc/Hz |
| Floor Fractional Mode | | | −226 | | dBc/Hz |
| Flicker (Both Modes) | | | −268 | | dBc/Hz |
| **VCO CHARACTERISTICS** | | | | | |
| VCO Tuning Sensitivity at RFOUT | Measured with 1.65 V on VTUNE | | | | |
| 7000MHz | | | 113 | | MHz/V |
| 9000 MHz | | | 80 | | MHz/V |
| 11000 MHz | | | 128 | | MHz/V |
| 13000 MHz | | | 109 | | MHz/V |
| 15000 MHz | | | 94 | | MHz/V |
| | | | | | |
| | | | | | |
| Tune Port Capacitance | Vtune = 0.5 Vdc / 1.65 Vdc / 2.8 Vdc | | 175 / 154 / 135 | | pF |
| VCO Supply Pushing[16] | Measured with 1.65 V on VTUNE | | | | MHz/V |
| | | | | | |

[1] Measured with 100 Ω external termination. See the Reference Input Stage section for more details.
[2] Slew rate of ≥0.5 ns/V is recommended. See the Reference Input Stage section for more details. Frequency is guaranteed across process voltage and temperature from −40°C to +85°C.
[3] This maximum PD frequency can only be achieved if the minimum N value is respected. For example, in the case of fractional mode, the maximum PD frequency = $f_{VCO}$/20 or 100 MHz, whichever is less.

[5] Limited by the 1 kΩ pull-up resistor and NMOS $R_{ON}$.
[6] 10 pF load capacitor.
[7] 10 pF load capacitor, 1 kΩ pull-up resistor. In general, open-drain mode can support higher frequencies at the expense of maximum $V_{OL}$. The maximum frequency for a given pull-up resistor and load capacitor is approximately $1/(10 \times R_{PULL\text{-}UP} \times C_{LOAD})$. For example, a 10 pF load capacitor and 1 kΩ pull-up resistor can support up to 10 MHz, where $V_{OL}$ maximum = $V_{DD} \times R_{ON}/(1\ k\Omega + R_{ON}) \approx 164$ mV. With a 500 Ω pull-up resistance and a 10 pF load, a 20 MHz maximum frequency is possible, and the maximum $V_{OL}$ increases to 300 mV.
[8] 1 kΩ pull-up resistor.
[9] The minimum resistive load to ground in CMOS mode is 1 kΩ.
[10] The LD/SDO pin does not have short-circuit protection. The maximum current of 7.2 mA must not be exceeded under any condition.
[11] $C_{LOAD}$ in pF. $C_{LOAD}$ maximum = 20 pF.
[12] VCCPD and VDDLS can be operated at 3.6 V maximum to increase band / VCO core overlap and extend upper end of frequency range, typical current at is expected to be less than 1.5mA. Both must be equal so if one changes so must the other. Exceeding 3.6 V results in ESD diodes drawing current.
[13] Reference disconnected.
[14] Some circuits remain on.
[15] Some circuits remain on.
[16] Pushing refers to a change in VCO frequency due to a change in the power supply voltage.

## TIMING SPECIFICATIONS

### *SPI Write Timing Characteristics*

AVDD = DVDD = 3 V, exposed pad (EP) = 0 V. See Figure 30.

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_1$ | SDI setup time to SCK rising edge | 3 | | | ns |
| $t_2$ | SCK rising edge to SDI hold time | 3 | | | ns |
| $t_3$ | SEN low duration | 10 | | | ns |
| $t_4$ | SEN high duration | 10 | | | ns |
| $t_5$ | SCK 32nd rising edge to SEN rising edge | 10 | | | ns |

| | | | | |
|---|---|---|---|---|
| $t_6$ | Recovery time | 20 | | ns |
| $f_{SCK}$ | Maximum serial port clock speed | | 50 | MHz |

### *SPI Read Timing Characteristics*

AVDD = DVDD = 3 V, exposed pad (EP) = 0 V. See Figure 31.

**Table 3.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_1$ | SDI setup time to SCK rising edge | 3 | | | ns |
| $t_2$ | SCK rising edge to SDI hold time | 3 | | | ns |
| $t_3$ | SEN low duration | 10 | | | ns |
| $t_4$ | SEN high duration | 10 | | | ns |
| $t_5$[1] | SCK rising edge to SDO time | | | 8.2 ns + 0.2 ns/pF | ns |
| $t_6$ | Recovery time | 10 | | | ns |
| $t_7$ | SCK 32$^{nd}$ rising edge to SEN rising edge | 10 | | | ns |

[1] An extra 0.2 ns delay is required for every 1 pF load on SDO.

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| $DV_{DD}$, $AV_{DD}$ to GND | −0.3 V to +3.6 V |
| $AV_{DD}$ to $DV_{DD}$ | −0.5V to +0.5 V |
| VDDLS, VPPCP to GND | −0.3 V to +3.8 V |
| VDDLS to VPPCP | −0.5V to +0.5 V |
| RVDD,VDDPD, VCCPS,VCCHF to GND | −0.3 V to +3.6 V |
| XREFP | +18dBm, 5.6V peak |
| Digital Load | 1.0 kOhm min |
| Digital Input 1.4V to 1.7V min rise time | 20 nsec |
| Digital Input Voltage Range | −0.25 V to $DV_{DD}$ + 0.5 V |
| VDD1, VDD2, VDD3 | −0.3 V to +3.6 V |
| VCCVCO | −0.3 V to +5.25V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +125°C |
| Maximum Junction Temperature | 150°C |
| $\theta_{JC}$, Thermal Impedance Junction to Case (ground paddle) | 6.9 °C/W |
| $\theta_{JA}$, Thermal Impedance Paddle Soldered to GND | 31.2 °C/W |
| Reflow Soldering | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 40 sec |
| Electrostatic Discharge (ESD) | |
| Charged Device Model | 500 V |
| Human Body Model | 1000 V |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## RECOMMENDED OPERATING CONDITIONS

**Table 5. Recommended Operating Conditions**

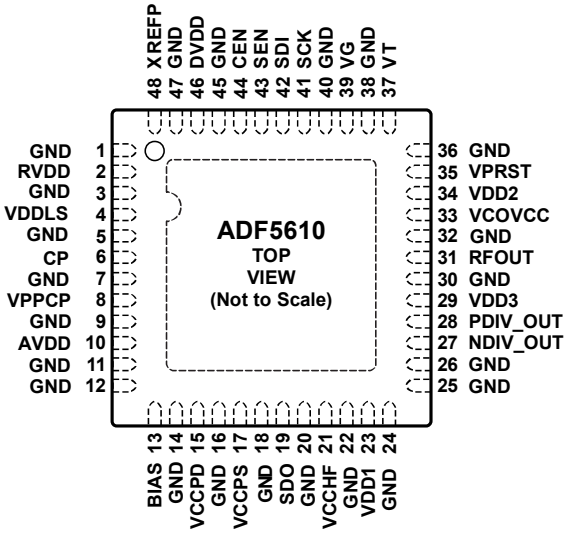
| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Temperature | | | | |
| Junction Temperature | | | 125 | °C |
| Ambient Temperature | −40 | | +85 | °C |
| Supply Voltage | | | | |
| AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS, VPPCP[1], VDDLS[1], VCC1, VCC2 | 3.1 | 3.3 | 3.5 | V |

[1]VPPCP and VDDLS may safely be operated at 3.6V.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




**NOTES**
**1. THE LGA HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS AND TO GND.**

*Figure 2. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1,3, 5, 7, 9, 11, 12, 14, 16,18, 20, 22 , 24 - 26, 30, 32, 36, 38, 40, 47 | GND | Ground |
| 2 | RVDD | Reference path supply, +3.3V ±5 % |
| 4 | VDDLS | Power supply for charge pump digital section, 3.3V, ± 5% typical, 3.6V ± 5% maximum, must be equal to VPPCP |
| 6 | CP | Charge Pump output. Place first pole of low pass loop filter close to this pin if loop filter path is electrically long. |
| 8 | VPPCP | Power supply for charge pump, 3.3V ± 5% typical, 3.6 V ± 5% maximum, must be equal to VDDLS |
| 10 | AVDD | Analog supply, 3.3Vdc ± 5%, must be equal to DVDD |
| 13 | BIAS | External Bypass Decoupling for Precision Bias Circuits. Note: 1.920 V ± 20 mV reference voltage (BIAS) is generated internally and cannot drive an external load. It must be measured with a 10 GΩ meter, such as the Agilent 34410A; a normal 10 MΩ DVM reads erroneously. |
| 15 | VCCPD | Phase Detector supply, 3.3V ± 5% |
| 17 | VCCPS | Prescaler supply, 3.3V ± 5% |
| 19 | SDO | Serial Data Output, lock detect and various other functions are available via internal MUX |
| 21 | VCCHF | Power supply for PLL RF section, 3.3V . A decoupling capacitor should be located as close as possible to this pin. |
| 23 | VDD1 | VCO digital logic supply, also provides bias input buffer to PLL, nominally 3.3V ± 5% |
| 27 | NDIV_OUT | Complementary output of differential frequency divider, N = 1,2,4,8,16,32,64 or128, DC block required, a broadband 100nF capacitor is recommended |
| 28 | PDIV_OUT | Primary output of differential frequency divider, N = 1,2,4,8,16,32,64, or 128 or DC block required, a broadband 100nF capacitor is recommended |
| 29 | VDD3 | Differential output divider supply, 3.3Vdc ± 5% |
| 31 | RFOUT | RF output (7.0GHz to 15.0GHz), DC block using a broadband 100nF capacitor. |
| 33 | VCOVCC | VCO power supply, 5.0V ± 5% |

| | | |
|---|---|---|
| 34 | VDD2 | Reference voltage supply , 3.3V ± 5% |
| 35 | VPRST | Temperature dependent, calibration preset. Decouple with a 470nF capacitor. |
| 37 | VT | VCO tuning port, 0 to 3.6 V ± 5%. Place last pole of low pass filtered charge pump output close to this pin if loop filter path is electrically long. |
| 39 | VG | Gate voltage bypassing, decouple to GND with a low ESR, 10uF capacitor |
| 41 | SCK | Serial Port Interface clock input |
| 42 | SDI | Serial Port Data Input |
| 43 | SEN | Serial Port Interface enable input, active high |
| 44 | CEN | Hardware chip enable input; active high. Logic low powers down PLL section |
| 46 | DVDD | Digital power supply, 3.3V ± 5% |
| 48 | XREFP | External reference input. For 50 ohm match, AC couple to XREFP pin using a low reactance capacitor value and add a shunt 100 ohm resistor to ground. |
| | EP | Exposed pad. The exposed pad or ground paddle on the backside of the package must be tied to RF / DC ground |

# TYPICAL PERFORMANCE CHARACTERISTICS

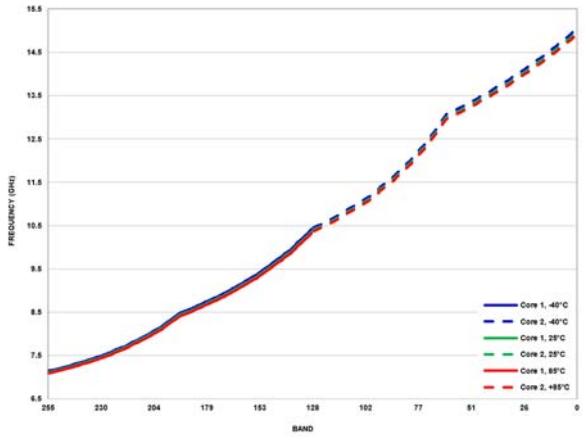



*Figure 3. Typical RFOUT Frequency vs VCO Band, Auto-Calibration Enabled, VDDLS = 3.3V, VPPCP = 3.3V*

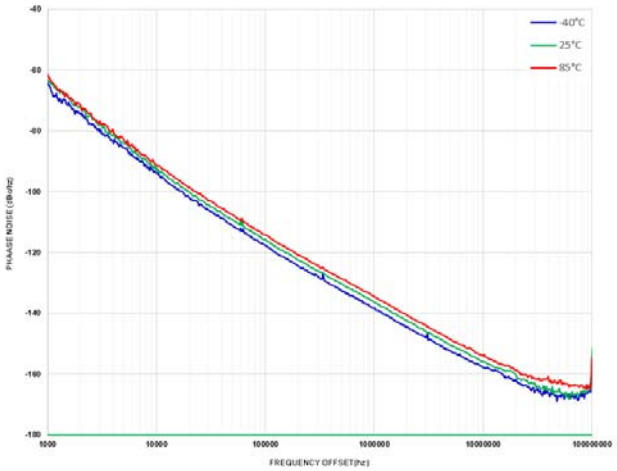



*Figure 4. Open-Loop VCO Phase Noise at 7000 MHz vs Temperature, RFOUT, High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

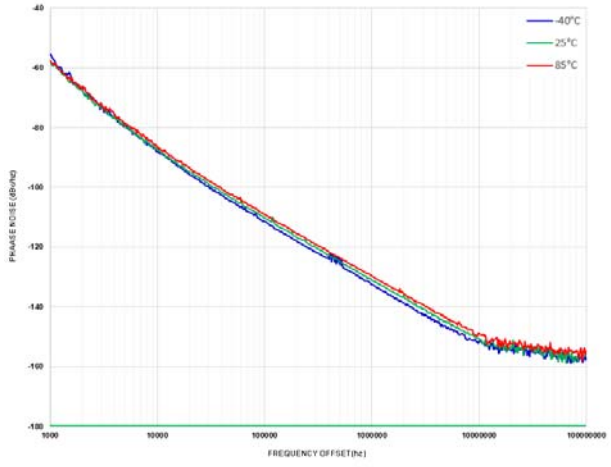



*Figure 5. Open-Loop VCO Phase Noise at 14800 MHz vs Temperature, RFOUT, High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

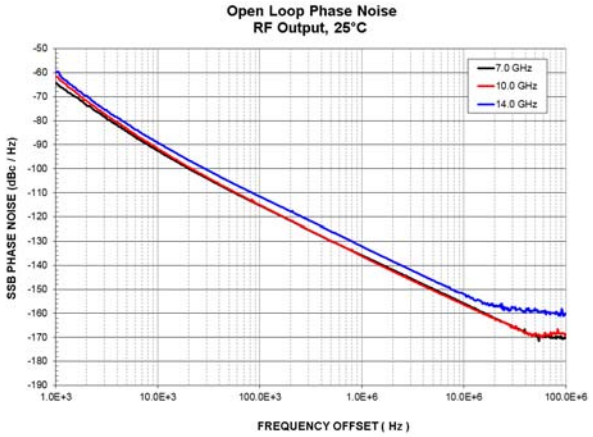



*Figure 6. Free Running VCO Phase Noise at 7.0 GHz, 10 GHz and 14 GHz, RFOUT, High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

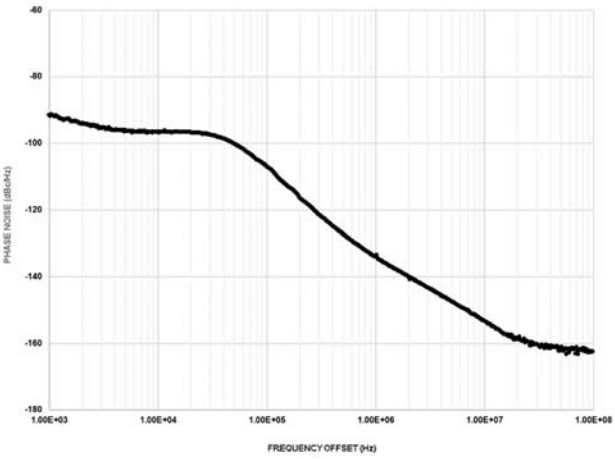



*Figure 7. Closed-Loop Phase Noise at 9.85 GHz, 50MHz VCXO Reference, 50MHz PFD, RFOUT, High Performance Mode (VCO_REG 0x01[4:2] = 7d), Agilent E5052B, 25°C*

*Figure 8.*

*Figure 9. Typical Closed-Loop Integer Phase Noise, 50 MHz PD Frequency, Output Gain = (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

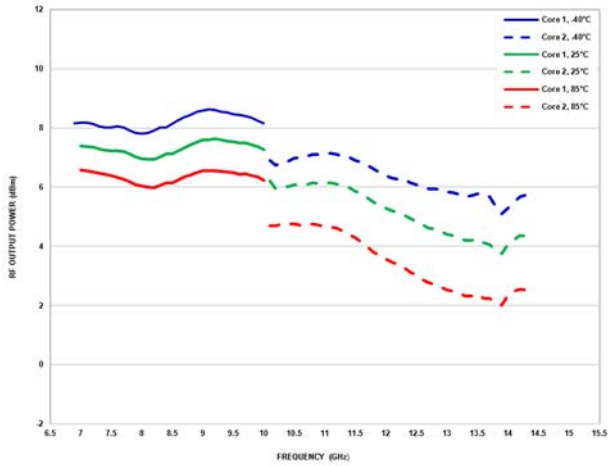



*Figure 10. RFOUT Output Power vs Temperature, Max Output Gain = (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

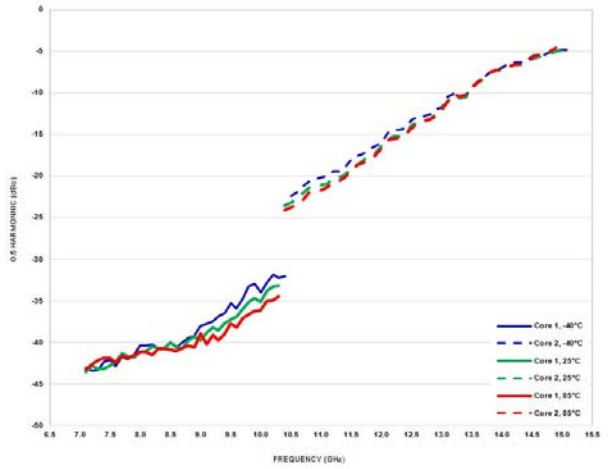



*Figure 11. RFOUT 0.5 Harmonic vs Temperature (Fundamental feedthrough at RFOUT), Max Output Gain = (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

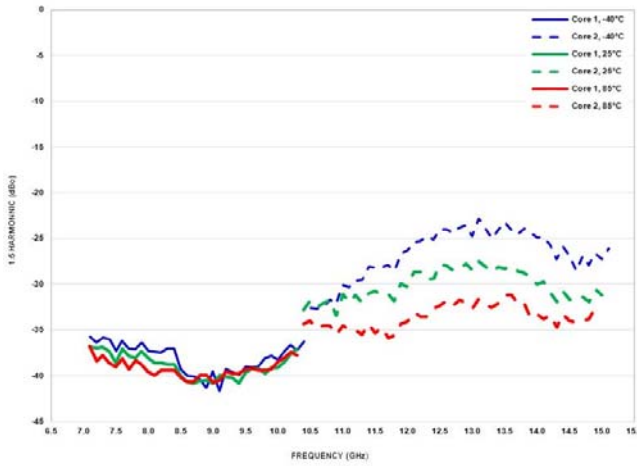



*Figure 12. 1.5 Harmonic vs Temperature, (3x Fundamental frequency vs RFOUT), Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

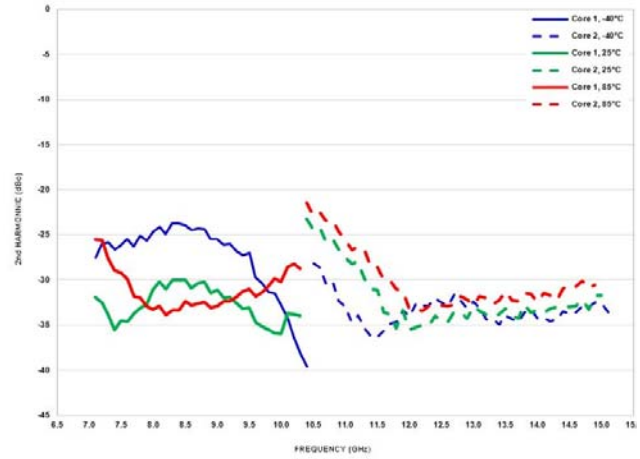



*Figure 13. RFOUT 2nd Harmonic vs Temperature, Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

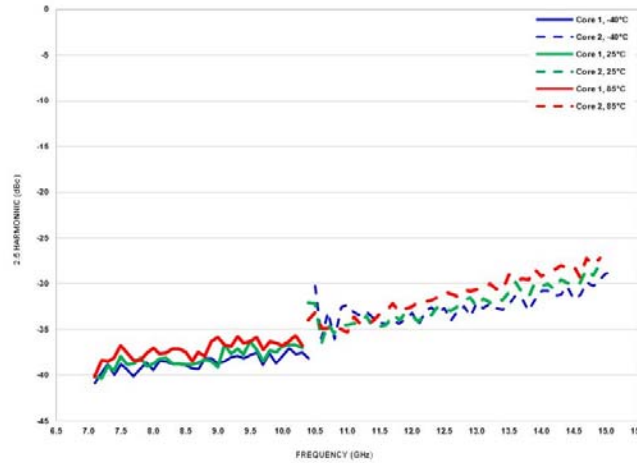



*Figure 14. 2.5 Harmonic vs Temperature, (5x Fundamental frequency vs RFOUT),*

*Max Output Gain (VCO_REG 0x01[1:0] = 3d),*
*High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

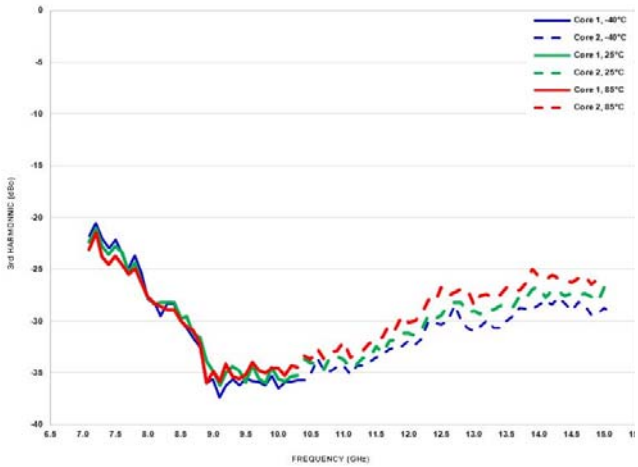



*Figure 15. 2.5 Harmonic vs Temperature, (5x Fundamental frequency vs RFOUT), Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

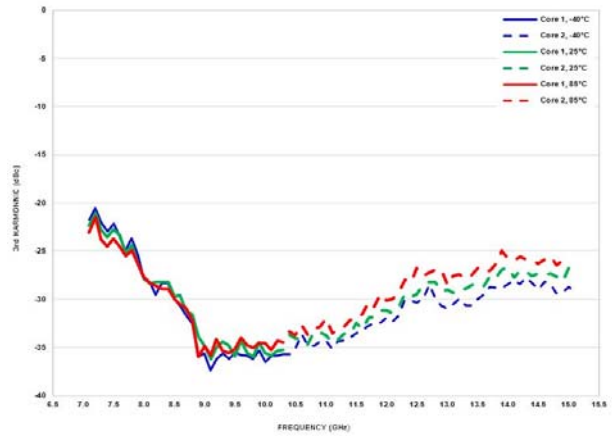



*Figure 16. 3rd Harmonic vs Temperature, Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

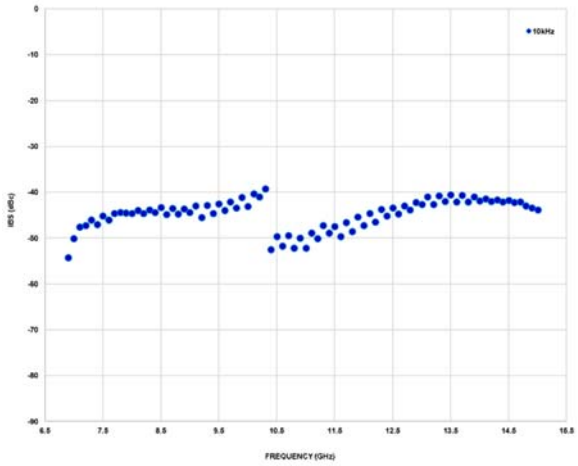



*Figure 17. 10kHz Integer Boundary Spur, 100kHz loop, 50MHz PFD, Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

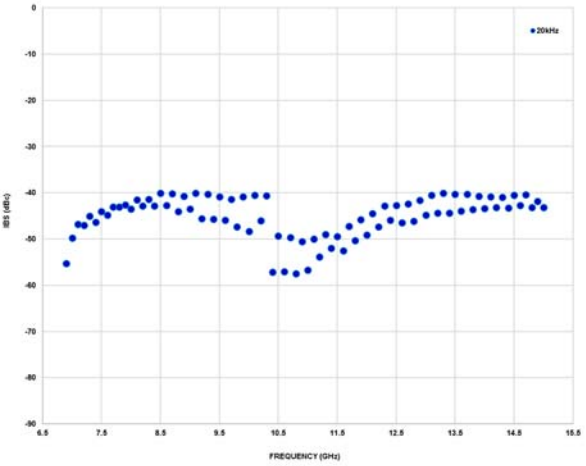



*Figure 18. 20kHz Integer Boundary Spur 100kHz loop, 50MHz PFD, Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

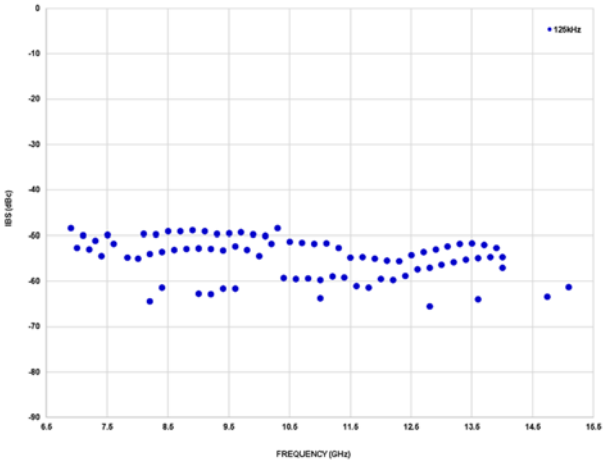



*Figure 19. 125kHz Integer Boundary Spur 100kHz loop, 50MHz PFD, Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

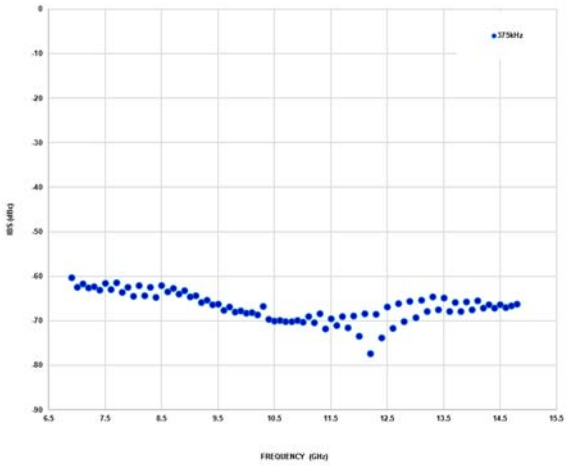



*Figure 20. 375kHz Integer Boundary Spur, 100kHz loop, 50MHz PFD, Max Output Gain (VCO_REG 0x01[1:0] = 3d), High Performance Mode (VCO_REG 0x01[4:2] = 7d)*

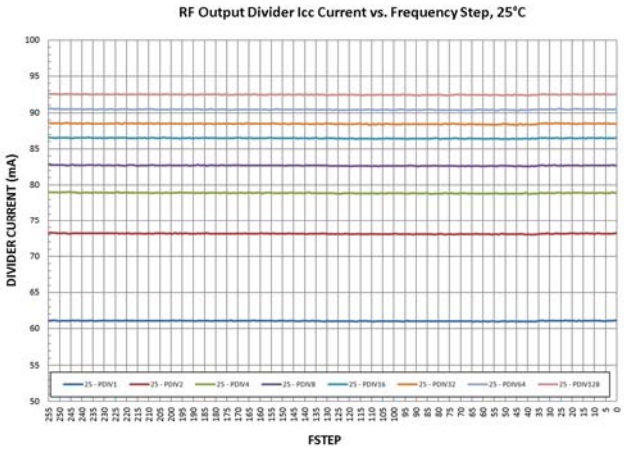



*Figure 21. Divider Current (VDD3) vs Divide Ratio vs VCO band, Max Divider Output Power (VCO_REG 0x01[6:5] = 3d, +25°C,*

# THEORY OF OPERATION

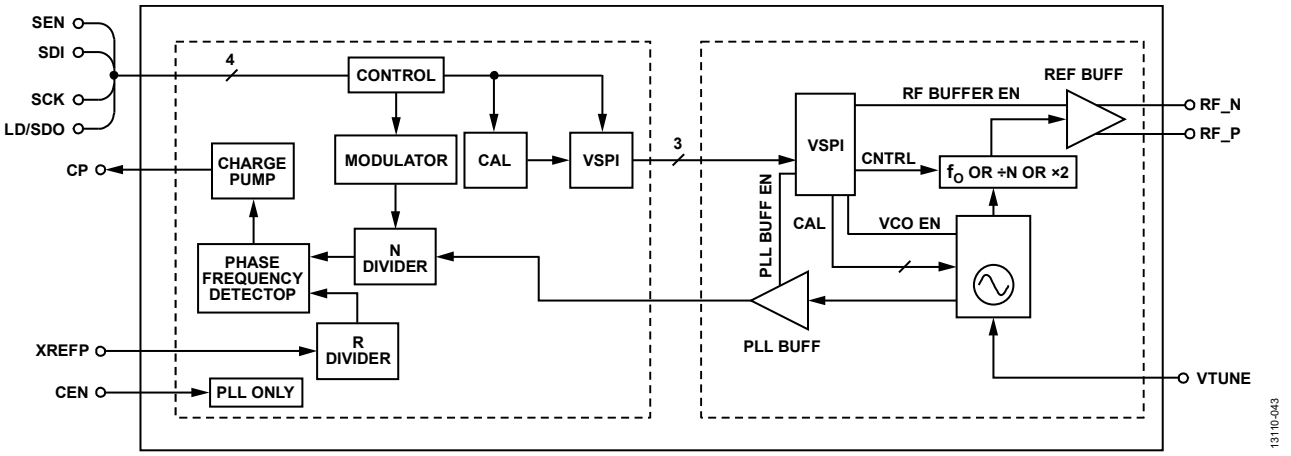



*Figure 22. PLL and VCO Subsystems*

The ADF5610 PLL with integrated VCO is composed of two subsystems: a PLL subsystem and a VCO subsystem, as shown in Figure 22.

## PLL SUBSYSTEM OVERVIEW

The PLL subsystem divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Register 0x03, fractional value set in Register 0x04), compares the divided VCO signal to the divided reference signal (reference divider set in Register 0x02) in the phase detector (PD), and drives the VCO tuning voltage via the charge pump (CP) (configured in Register 0x09) to the VCO subsystem. Some of the additional PLL subsystem functions include

- Σ-Δ configuration (Register 0x06).
- Exact frequency mode (configured in Register 0x0C, Register 0x03, and Register 0x04).
- Lock detect (LD) configuration (use Register 0x07 to configure LD and Register 0x0F to configure the LD/SDO output pin).
- External CEN pin used for the hardware PLL enable pin. The CEN pin does not affect the VCO subsystem.

Typically, only writes to the divider registers (integer part uses Register 0x03, fractional part uses Register 0x04) of the PLL subsystem are required for ADF5610 output frequency changes.

The divider registers of the PLL subsystem (Register 0x03 and Register 0x04) set the fundamental frequency (3500 MHz to 7000 MHz) of the VCO subsystem. Output frequencies ranging from 55 MHz to 15000 MHz are generated by tuning to the appropriate fundamental VCO frequency (3500 MHz to 7000 MHz) by programming the N divider (Register 0x03 and Register 0x04) and programming the output divider (divide by 1 to 128, in VCO_REG 0x02) in the VCO subsystem.

For detailed frequency tuning information and an example, see the Frequency Tuning section.

## VCO SUBSYSTEM OVERVIEW

The VCO subsystem consists of a capacitor switched, step tuned VCO and an output stage. During normal operation, the VCO subsystem is programmed with the appropriate capacitor switch setting that is executed automatically by the PLL subsystem autocalibration state machine when autocalibration is enabled (Register 0x0A[11] = 0; see the VCO Calibration section for more information). The VCO tunes to the fundamental frequency (3500 MHz to 7000 MHz), and is locked by the CP output from the PLL subsystem. The VCO subsystem controls the output stages of the ADF5610, enabling configuration of

- User defined performance settings (see the Programmable Performance Technology section) that are configured via VCO_REG 0x01[11:9].
- VCO output divider settings that are configured in VCO_REG 0x02[9:7] (divide by 2 to 128 to generate frequencies from 3500 MHz to 55 MHz respectively), or divide by 1 to generate frequencies between 7000 MHz and 15000 MHz.
- RFOUT  gain settings (VCO_REG 0x01[8:7]).
- PDIV / NDIV Gain settings (VCO_REG 0x1[13:12].
- Power Down VCO (VCO_REG 0x02[10].
- Power Down Divider (VCO_REG 0x01[15].

## SPI CONFIGURATION OF PLL AND VCO SUBSYSTEMS

The two subsystems (PLL subsystem and VCO subsystem) have their own register maps as shown in the PLL Register Map and VCO Subsystem Register Map sections. Typically, writes to both register maps are required for initialization and frequency tuning operations.

As shown in Figure 22, the PLL subsystem is connected directly to the SPI of the ADF5610, whereas the VCO subsystem is

connected indirectly through the PLL subsystem to the ADF5610 SPI. As a result, writes to the PLL register map are written directly and immediately, whereas the writes to the VCO subsystem register map are written to the PLL Register 0x05 and forwarded via the internal VCO SPI (VSPI) to the VCO subsystem. This is a form of indirect addressing.

VCO subsystem registers are write only and cannot be read. However, the VCO tuning band that is currently enabled may be read back via PLL REG 0x0A. For more information, see the VCO Serial Port Interface (VSPI) section below.

### *VCO Serial Port Interface (VSPI)*

The ADF5610 communicates with the internal VCO subsystem via an internal 16-bit VCO SPI. The internal serial port controls the step tuned VCO and other VCO subsystem functions.

The internal VSPI runs at the rate of the autocalibration finite state machine (FSM) clock, $t_{FSM}$ (see the VCO Autocalibration section), where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by PLL Register 0x0A[14:13].

Writes to the control registers of the VCO are handled indirectly via writes to Register 0x05 of the ADF5610. A write to Register 0x05 causes the internal PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where it is interpreted.

#### VSPI Use of Register 0x05

The packet data written into Register 0x05 is sub-parsed by logic at the VCO subsystem into the following three fields:

Field 1—Bits[2:0]: 3-bit VCO_ID, target subsystem address = 000b.

Field 2—Bits[6:3]: 4-bit VCO_REGADDR, the internal register address inside the VCO subsystem.

Field 3—Bits[15:7]: 9-bit VCO_DATA, the data field to write to the VCO register.

For example to write 0 0000 0110 into Register 2 of the VCO subsystem (VCO_ID = 000b), and set the VCO output divider to divide by 2, the following must be written to Register 0x05 = 0b(VCO_DATA [15]), 0000b(VCO_DATA [14:11]), 0110b (VCO_DATA [10:7]), 0010b (VCO_REGADDR), 000b (VCO_ID) or, equivalently, Register 0x05 = 0x0310.

During autocalibration, the autocalibration controller writes into the VCO register address specified by the VCO_ID and VCO_REGADDR, as stored in Register 0x05[2:0] and Register 0x05[6:3], respectively. Autocalibration requires that the values for the VCO_ID be zero (Register 0x05[6:0] = 0); when they are not zero (Register 0x05[6:0] ≠ 0), autocalibration does not function.

To ensure that the autocalibration functions, it is critical to write Register 0x05[6:0] = 0 after the last VCO subsystem write but prior to an output frequency change that is triggered by a write to either Register 0x03 or Register 0x04.

However, it is impossible to write only Register 0x05[6:0] = 0 (VCO_ID and VCO_REGADDR) without also writing VCO_DATA (Register 0x05[15:7]). Therefore, if it is desired to remain in the existing VCO band and only change the divide ratio (see previous example) we must ensure that VCO_DATA (Register 0x05[15:7]) is not changed. In order to accomplish this, it is required to read the switch settings provided in Register 0x10[7:0], and then rewrite them to Register 0x05[15:7], as follows:

1. Read Register 0x10.
2. Write to Register 0x05 the following:
    a. Register 0x05[15:14] = Register 0x10[7:6];
    b. Register 0x05[13] = 1 (reserved bit);
    c. Register 0x05[12:8] = Register 0x10[4:0];
    d. Register 0x05[7:0] = 0.

Changing the VCO subsystem configuration (see the VCO Subsystem Register Map section) without following the above procedure results in a failure to lock to the desired frequency.

For applications not using the read functionality of the ADF5610 SPI, in which Register 0x10 cannot be read, it is possible to write Register 0x05 = 0x0 to set Register 0x05[6:0] = 0, which also sets the VCO sub-band setting equal to zero (Register 0x05[15:7] = 0), effectively programming incorrect VCO sub-band settings and causing the ADF5610 to lose lock. This procedure is then immediately followed by a write to

- Register 0x03, if in integer mode
- Register 0x04, if in fractional mode

This write effectively re-triggers the autocalibration state machine, forcing the ADF5610 to relock whether in integer or fractional mode.

Lock time is typically in the order of 100 µs for a phase settling of 10°, and is dependent on both the loop filter design (loop filter bandwidth and loop filter phase margin) and the configuration of autocalibration (Reg 0x0A).

## VCO SUB-SYSTEM

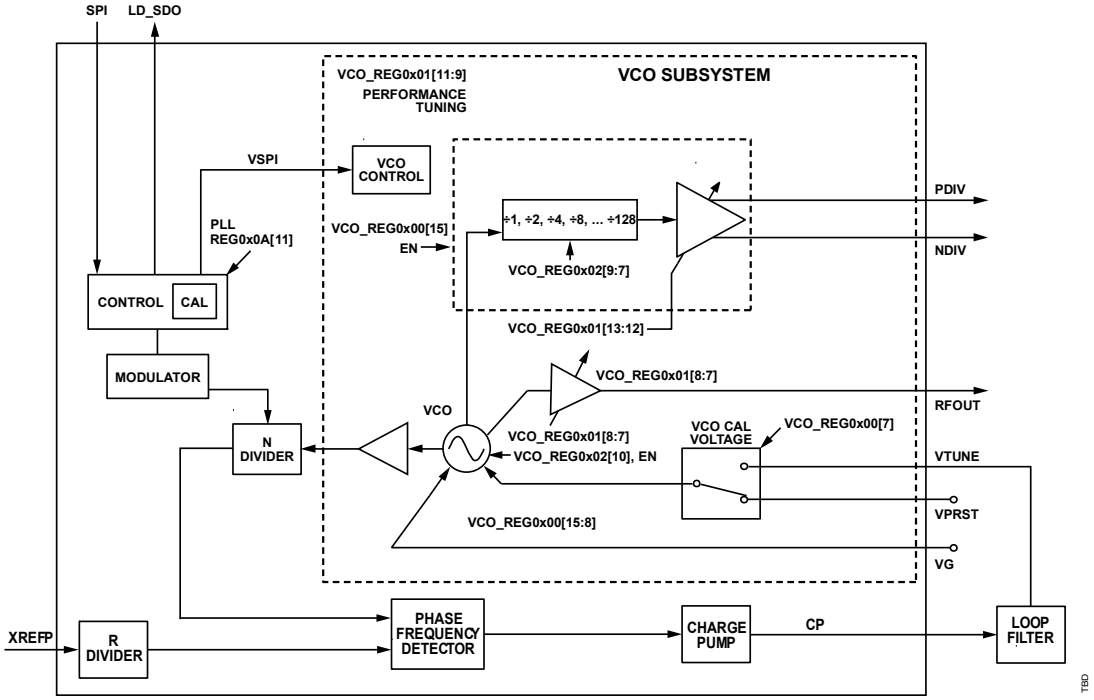



*Figure 23. PLL and VCO Subsystems*

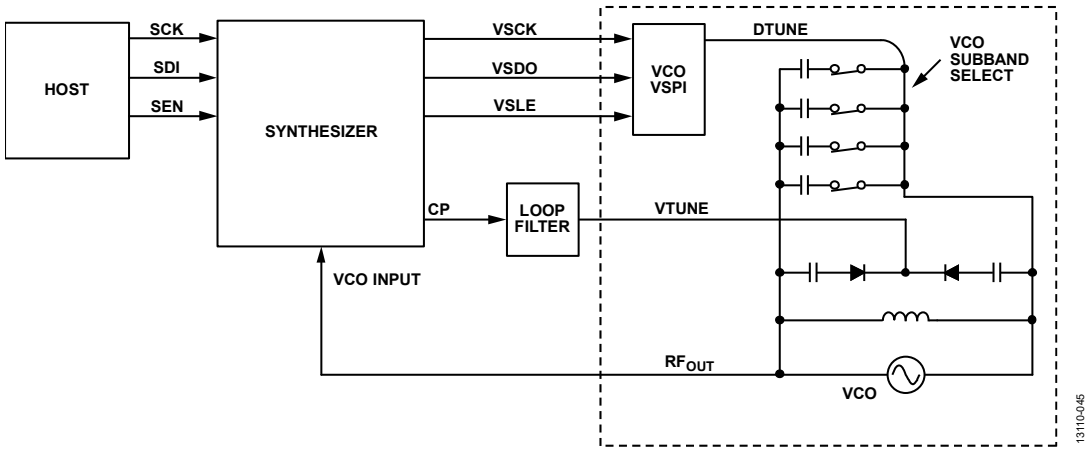



*Figure 24. Simplified Step Tuned VCO*

The ADF5610 contains a VCO subsystem that can be configured to provide the following output frequencies:

- Fundamental frequency (fo) mode (3500 MHz to 7000 MHz) is available at the differential outputs by setting the output frequency divider to N = 2.
- The push-push (doubled) frequency is always available at RFOUT. It's also available at the differential outputs by setting N = 1 to bypass the divider.
- Divide by N mode, where N = 1, 2, 4, 6, 8 … 32, 64, 128 (55 MHz to 1750 MHz).

All modes are VCO register programmable, as shown in Figure 23. One loop filter design can be used for the entire frequency of operation of the ADF5610.

### *VCO Calibration*

#### VCO Autocalibration

The ADF5610 incorporates a step tuned VCO. A simplified step tuned VCO is shown in Figure 24. Step tuned VCO's are

unique in that they incorporate not only varactor diodes for frequency tuning but also a digitally selectable, binary bank of capacitors. It is this bank of capacitors along with the varactor diodes that defines the frequency range of each sub-band within a given VCO core. The ADF5610 contains two VCO cores, each with their own bank of capacitors. Multiple VCO cores allow not only broader frequency coverage but also more consistent tuning sensitivity across the band.

As capacitors are selected or de-selected within the bank, the nominal center frequency of the VCO tank circuit is "stepped" up or down. Multiple capacitors may be changed at once or one at a time if required. Essentially, the capacitor banks provide "coarse" frequency tuning in the form of 128 sub-bands within each VCO core while the varactor diodes manage "fine" tuning within each of these sub-bands. To guarantee continuous frequency coverage over process, voltage and temperature (PVT) the ends of each frequency sub-band and each VCO core, overlap.

The frequency overlap implies that certain frequencies exist in more than one sub-band. It is well known that the frequency of a VCO varies (drifts) with temperature. Selection of a sub-band where the desired frequency is too close to the edge could lead to loss of lock if the operating temperature change is great enough and in a direction that will allow the frequency to drift beyond the edge of the sub-band. If automatic relock is enabled (REG 0x07[13] = 1, the autocalibration routine will run one additional time in an attempt to re-lock the synthesizer. Note that depending on the cause of the initial loss-of-lock a different band may be selected. The temporary loss-of-lock will result in a "phase hit" during this transition period. This is unacceptable for some applications. If a different band is selected upon re-lock, the tuning sensitivity will change slightly resulting in a minor shift to the 3 dB corner for the loop filter which may negatively impact phase settling time or spurious suppression. If the loss-of-lock was initially due to selection of a band where the frequency is near the band edge then the accompanying tuning voltage will be close to the charge pump rail. As the charge pump approaches its limits of operation (rails) its performance becomes non-linear resulting in increased spurious and PLL figure of merit (FOM) and consequently degrades phase noise performance at frequency offsets inside the loop filter bandwidth.

The ADF5610 simultaneously solves these potential issues by integrating a temperature compensation circuit within the autocalibration routine. This circuit produces a very low noise, temperature dependent voltage and depending on the state of the autocalibration bit (VCO_REG 0x0[7] routes it to the tuning port of the VCO. When the operating temperature of the ADF5610 is low (-40°C), a band where the desired frequency will occur at a low tune voltage is required so that as the temperature increases, higher tune voltages are available. Likewise, when the ADFD5610 is operating at high temperatures (+85°C) a band where the desired frequency falls at a higher tune voltage is needed in order to maintain lock as the temperature drops. The reference voltage used for band selection ranges linearly from about 0.85 Vdc at -40°C to 1.75 Vdc at +85°C. The voltage range which is centered around 1.3 Vdc at room temperature is offset with respect to the available tune voltage range of 0 Vdc to 3.3 Vdc. This allows additional voltage at the upper end of each VCO core to compensate for the reduction in tuning sensitivity. By limiting the voltage range from approximately 0.85 Vdc to 1.70 Vdc, bands will be selected that allow operation well away from the charge pump rails over the full operating temperature range. This guarantees that bands will be selected that allow "lock and leave" performance. That is, phase lock is maintained within a single VCO core and VCO sub-band over the full temperature range (-40°C to +85°C) regardless of the operating temperature when autocalibration initially selected the sub-band.

When the ADF5610 PLL receives a request to change the frequency such that a new VCO band must be selected, the process is as follows. Note that the PLL portion of the autocalibration circuitry, the finite state machine (FSM), is assumed to already be enabled (REG 0x0A[11] = 0).

1) The PLL registers that must be updated in order to facilitate lock at the new frequency as well as any changes to the VCO registers (gain settings, divide ratio,...) are set to the ADF5610 via the SPI interface. Note that the VCO autocalibration bit should not be changed. Its state is handled automatically when PLL REG 0x0A[11] = 0.
2) The FSM takes control of the VCO autocalibration bit (VCO_REG 0x0[7] changing it from '0' to '1' temporarily opening the loop filter path and switching the source of the VCO tune voltage (VT) from the charge pump to the temperature compensated tune voltage (VPRST).
3) Now, with VT set to a value that will provide optimal performance, the PLL state machine begins a binary search for the VCO core and sub-band with a frequency that is closest to the desired frequency.
    a. Note that the setting for the VTUNE resolution (REG0x0A[2:0]) can impact band selection as well as the ability to retain lock over the full operating temperature range. When in doubt use the highest setting for the best resolution.
4) Once the proper band has been determined, the VCO Auto-Calibration bit (VCO_REG 0x0[7] changes from

'1' back to '0' closing the loop filter path and returning the source of the VCO tune voltage (VT) to the charge pump.

5) The new VCO frequency is now routed to the input of the PLL, divided down and compared to the reference frequency. The charge pump adjusts the VCO tuning voltage as necessary to lock phase lock the new frequency to the reference frequency.

The temperature compensated voltage that is used during autocalibration is brought out to the VPRST pin (pin 35) of the ADF5610. This could be useful for a real time estimate of the junction temperature of the die however some caution should be exercised if it is desired to continuously monitor this voltage. This is a low noise circuit and although the internal switch has good isolation, it could still allow external noise to be coupled onto the precision reference circuit which would result in unwanted spurs, sidebands and degraded phase noise.

Although the digital VCO switches are normally automatically controlled by the ADF5610 using the autocalibration feature, the VCO switches can also be controlled directly via Register 0x05 for testing or for special purpose operations. Other control bits specific to the VCO are also sent via Register 0x05. Refer to the VCO Subsystem Register Map section for further details.

As mentioned previously, during autocalibration, coarse tuning is provided by the FSM as it selects the most appropriate band for operation over the full operating temperature range. Fine tuning is achieved by varactor diodes once the VCO autocalibration bit VCO_REG 0x0[7] is reset by the FSM. This gives control of the tuning voltage back to the phase detector and charge pump. Since the band has been selected, a narrow arrow voltage range on the varactor is all that is needed for phase lock. Note that the tuning voltage stays in a narrow range over a wide range of output frequencies.

The calibration is normally run automatically, once for every change of frequency. This autocalibration ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally need to be concerned about which switch setting is used for a given frequency because this is handled by the autocalibration routine.

The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency and ensures that the VCO stays locked and performs well over its full temperature range without additional calibration, regardless of the temperature at which the VCO was calibrated.

Autocalibration can also be disabled, thereby allowing manual VCO tuning. Refer to the Manual VCO Calibration for Fast Frequency Hopping section for more information about manual tuning.

### Autocalibration Using Register 0x05

Autocalibration transfers switch control data to the VCO subsystem via Register 0x05. The address of the VCO subsystem in Register 0x05 is not altered by the autocalibration routine. The address and ID of the VCO subsystem in Register 0x05 must be set to the correct value before autocalibration is executed. For more information, see the VCO Serial Port Interface (VSPI) section.

### Automatic Relock on Lock Detect Failure

It is possible, by setting Register 0x07[13], to have the VCO subsystem automatically rerun the calibration routine and relock itself if the lock detect indicates an unlocked condition for any reason. With this option, the system attempts to relock only once.

### VCO Autocalibration on Frequency Change

Assuming Register 0x0A[11] = 0, the VCO calibration starts automatically whenever a frequency change is requested. To rerun the autocalibration routine for any reason at the same frequency, rewrite the frequency change with the same value, and the autocalibration routine executes again without changing the final frequency.

### VCO Autocalibration Time and Accuracy

The VCO frequency is counted for $t_{MMT}$, the period of a single autocalibration measurement cycle.

$$t_{MMT} = t_{XTAL} \times R \times 2^n \quad (1)$$

where:

$t_{XTAL}$ is the period of the external reference (crystal) oscillator.
$R$ is the reference path division ratio currently in use, set in Register 0x02.

$n$ is set by Register 0x0A[2:0] and results in measurement periods that are multiples of the PD period, $t_{XTAL} \times R$.

The VCO autocalibration counter, on average, expects to register N counts, rounded down (floor) to the nearest integer, for every PD cycle.

N is the ratio of the target VCO frequency, $f_{VCO}$, to the frequency of the PD, $f_{PD}$, where N can be any rational number supported by the N divider.

N is set by the integer and fractional register contents using Equation 2.

$$N = N_{INT} + N_{FRAC}/2^{24} \quad (2)$$

where:
$N_{INT}$ is the integer set in Register 0x03.
$N_{FRAC}$ is the fractional part set in Register 0x04.

The autocalibration state machine and the data transfers to the internal VCO VSPI run at the rate of the FSM clock, $t_{FSM}$, where the FSM clock frequency cannot be greater than 50 MHz.

$$t_{FSM} = t_{XTAL} \times 2^m \quad (3)$$

where $m$ is 0, 2, 4, or 5 as determined by Register 0x0A[14:13].

The expected number of VCO counts, V, is given by

$$V = floor\ (N \times 2^n) \quad (4)$$

The nominal VCO frequency measured, $f_{VCOM}$, is given by

$$f_{VCOM} = \mathrm{V} \times f_{XTAL}/(2^n \times R) \quad (5)$$

where the worst case measurement error, $f_{ERR}$, is

$$f_{ERR} \approx \pm f_{PD}/2^{n+1} \quad (6)$$

For example, the autocalibration time (tcal) for an 8-bit step tuned VCO (where the total number of bits includes those needed to switch VCO cores) is as follows. First a 20 * (k+1) bit wait state occurs. The measurement has a programmable number of wait states, k, of 128 FSM cycles defined by Register 0x0A[7:6] = k. Wideband VCO's like the ADF5610 require additional wait time (typically, k = 1) whereas narrowband VCO's may be fine setting k =0. The wait period is followed by the measurement time (Tmmt) for calibration then VSPI data transfers of 20 clock cycles each. This repeats 8 times since we have 1 bit to select the VCO core and 7 bits to select the VCO band for a total of 8 bits. Total calibration time, worst case, is given by

$$t_{CAL} = k128\ t_{FSM} + 8t_{PD}\ 2^n + 8 \times 20\ t_{FSM} \quad (7)$$

or equivalently

$$t_{CAL} = t_{XTAL}\ (8R \times 2^n + (160 + (k \times 128)) \times 2^m) \quad (8)$$

For guaranteed hold of lock, across temperature extremes, the resolution must be better than 1/8th of the frequency step caused by a VCO sub-band switch change. Better resolution settings show no improvement.

### VCO Autocalibration Example

The VCO subsystem must satisfy the maximum $f_{PD}$ limited by the two following conditions:

$$N \geq 16\ (f_{INT}),\ N \geq 20.0\ (f_{FRAC})$$

where:
$N = f_{VCO}/f_{PD}$. $f_{PD} \leq 100$ MHz.
$f_{INT}$ is integer mode.
$f_{FRAC}$ is fractional-N mode. The minimum N values changes depending on the operating mode.

For example, if the VCO subsystem output frequency is to operate at 7.01 GHz and the crystal frequency is $f_{XTAL}$ = 50 MHz, R = 1, and m = 2 (see Figure 25), then $t_{FSM}$ = 80 ns (12.5 MHz).

When using autocalibration, the maximum autocalibration FSM clock cannot exceed 50 MHz (see Register 0x0A[14:13]). The FSM clock does not affect the accuracy of the measurement; it only affects the time to produce the result. This same clock clocks the 16-bit VCO serial port.

If the time to change frequencies is not a concern, the calibration time for maximum accuracy can be set and, therefore, the measurement resolution is of no concern.

Using an input crystal of 50 MHz (R = 1 and $f_{PD}$ = 50 MHz), the times and accuracies for calibration using Equation 6 and Equation 8 are listed in Table 7, where minimal tuning time is 1/8th of the VCO band spacing.

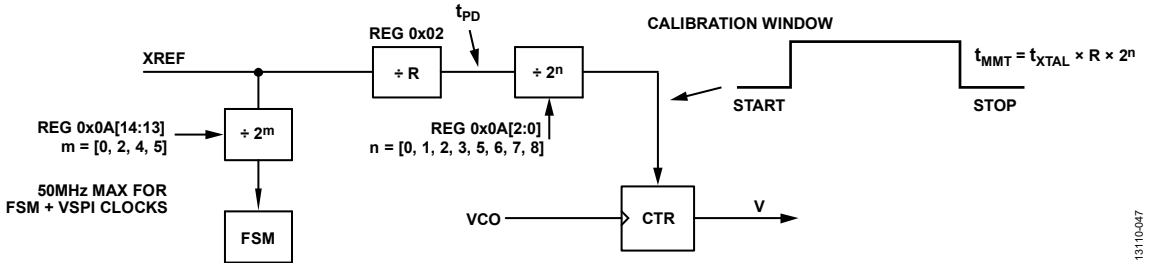



*Figure 25. VCO Calibration*

**Table 7. Auto-calibration Example with $f_{XTAL}$ = 50 MHz, R = 1, m = 2**

| Control Value Register 0x0A[2:0] | n | $2^n$ | $t_{MMT}$ (µs) | $t_{CAL}$ (µs) | $f_{ERR}$ Maximum |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0.02 | 33.44 | ±25 MHz |
| 1 | 1 | 2 | 0.04 | 33.60 | ±12.5 MHz |
| 2 | 2 | 4 | 0.08 | 33.92 | ±6.25 MHz |
| 3 | 3 | 8 | 0.16 | 34.56 | ±3.125 MHz |
| 4 | 5 | 32 | 0.64 | 38.40 | ±781 kHz |

| Control Value Register 0x0A[2:0] | n | $2^n$ | $t_{MMT}$ (µs) | $t_{CAL}$ (µs) | $f_{ERR}$ Maximum |
|---|---|---|---|---|---|
| 5 | 6 | 64 | 1.28 | 43.52 | ±390 kHz |
| 6 | 7 | 128 | 2.56 | 53.76 | ±95 kHz |
| 7 | 8 | 256 | 5.12 | 74.24 | ±98 kHz |

Across all VCOs, a measurement resolution better than 800 kHz produces correct results. Setting m = 2 and n = 5 provides 781 kHz of resolution and adds 38.4 µs of autocalibration time to a normal frequency hop. After the autocalibration sets the final switch value, 38.4 µs after the frequency change command, the fractional register is loaded, and the loop locks with a normal transient predicted by the loop dynamics. Therefore, as shown in this example, autocalibration typically adds about 38.4 µs to the normal time to achieve frequency lock. Use autocalibration for all but the most extreme frequency hopping requirements.

**Manual VCO Calibration for Fast Frequency Hopping**

When switching frequencies quickly is needed, it is possible to eliminate the autocalibration time by calibrating the VCO in advance and storing the switch number vs. frequency information in the host, which is accomplished by initially locking the ADF5610 on each desired frequency using autocalibration, then reading and storing the selected VCO switch settings. The VCO switch settings are available in Register 0x10[7:0] after every autocalibration operation. The host must then program the VCO switch settings directly when changing frequencies.

Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when autocalibration is disabled. Therefore, frequency changes with manual control and autocalibration disabled requires a minimum of two serial port transfers to the PLL, once to set the VCO switches and once to set the PLL frequency.

When autocalibration is disabled (Register 0x0A[11] = 1), the VCO updates its registers immediately with the value written via Register 0x05. The VCO internal transfer requires 16 VSCK clock cycles after the completion of a write to Register 0x05. VSCK and the autocalibration controller clock are equal to the input reference divided by 0, 4, 16, or 32 as controlled by Register 0x0A[14:13].

For settling time requirements faster than 1 ms, contact Analog Devices, Inc., applications support. Settling times under 100 µs are possible but certain conditions on performance do exist.

***Registers Required for Frequency Changes in Fractional Mode***

In fractional mode (Register 0x06[11] = 1), a large change of frequency may require main serial port writes to one of the three following registers:

- The integer register, Register 0x03. This write is required only if the integer part changes.
- The VCO SPI register, Register 0x05. This write is required only for manual control of VCO if Register 0x0A[11] = 1, autocalibration is disabled, or to change the VCO output divider value (VCO_REG 0x02). See Figure 23 for more information.
- The fractional register, Register 0x04. The fractional register write triggers autocalibration when Register 0x0A[11] = 0, and it is loaded into the modulator automatically after the autocalibration runs. If autocalibration is disabled, Register 0x0A[11] = 1, the fractional frequency change is loaded immediately into the modulator when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with autocalibration enabled (Register 0x0A[11] = 0), usually require only a single write to the fractional register. In a worst case scenario, three main serial port transfers to the ADF5610 may be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register, Register 0x04, for frequency changes.

***Registers Required for Frequency Changes in Integer Mode***

In integer mode (Register 0x06[11] = 0), a change of frequency requires main serial port writes to the following registers:

- VCO SPI register, Register 0x05. This write is required only for manual control of the VCO when Register 0x0A[11] = 1 (autocalibration disabled) or when the VCO output divider value must change (VCO_REG 0x02).
- Integer register, Register 0x03. In integer mode, an integer register write triggers autocalibration when Register 0x0A[11] = 0 and it is loaded into the prescaler automatically after autocalibration runs. If autocalibration is disabled, Register 0x0A[11] = 1, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally, changes to the integer register cause large steps in the VCO frequency; therefore, the VCO switch settings must be adjusted. Autocalibration enabled is the recommended method for integer mode frequency changes. If autocalibration is disabled (Register 0x0A[11] = 1), a prior knowledge of the correct VCO switch setting and the

corresponding adjustment to the VCO is required before executing the integer frequency change.

### *VCO Built-In Self Test (BIST) with Autocalibration*

The frequency limits of the VCO can be measured using the BIST features of the autocalibration machine by setting Register 0x0A[10] = 1, which freezes the VCO switches in one position. VCO switches can then be written manually with the varactor biased at the nominal mid-rail voltage used for autocalibration. For example, to measure the VCO maximum frequency, use Switch 0, written to the VCO subsystem via Register 0x05 = 000000001 0000 VCO_ID, where VCO_ID = 000b.

When autocalibration is enabled (Register 0x0A[11] = 0), and a new frequency is written, autocalibration runs. The VCO frequency error relative to the command frequency is measured and the results are written to Register 0x11[19:0], where Register 0x11[19] is the sign bit. The result is written in terms of VCO count error (see Equation 4).

For example, if the expected VCO frequency is 7.0 GHz, the reference is 50 MHz, and REG 0x0A[2:0] = 8 (n =8) expect to measure $3500/(50/2^8) = 17920$ counts. Frequencies less than 8.0GHz route the fundamental frequency directly to the N counter so in this case 3500MHz is routed to the N Counter. For RFOUT frequencies greater than or equal to 8.0 GHz the internal prescaler of the PLL (REG 0x08[19]) must be enabled. If a difference of −5 counts is measured in Register 0x11, it means 17915 counts were actually measured. With a 7 GHz VCO, 50 MHz reference, and n = 8, one count is approximately ±195.3 kHz. Therefore, the actual frequency of the VCO is 5 / 17920 low (negative), for a fundamental frequency of 3499.0234375 MHz or push-push frequency of 6998.04687 MHz at RFOUT.

## PLL SUBSYSTEM

### *Charge Pump (CP) and Phase Detector (PD)*

The phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock, these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. The frequency of operation of the PD is $f_{PD}$. Most formulas related to, for example, step size, Σ-Δ modulation, and timers, are functions of the operating frequency of the PD, $f_{PD}$. $f_{PD}$ is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

**Charge Pump**

A simplified diagram of the charge pump is shown in Figure 26. The CP consists of four programmable current sources: two controlling the CP gain (up gain, Register 0x09[13:7], and down gain, Register 0x09[6:0]) and two controlling the CP offset, where the magnitude of the offset is set by Register 0x09[20:14], and the direction is selected by Register 0x09[21] = 1 for up offset and Register 0x09[22] = 1 for down offset.

CP gain is used at all times, whereas CP offset is recommended for fractional mode of operation only. Typically, the CP up and down gain settings are set to the same value (Register 0x09[13:7] = Register 0x09[6:0]).

**Charge Pump Gain**

Charge pump up and down gains are set by Register 0x09[13:7] and Register 0x09[6:0], respectively. The current gain of the pump in amps/radian is equal to the gain setting of this register (Register 0x09) divided by 2π.

The typical CP gain setting is set from 2 mA to 2.5 mA; however, lower values can also be used. Note that values less than 1 mA may result in degraded phase noise performance.

For example, if both Register 0x09[13:7] and Register 0x09[6:0] are set to 50 decimal, the output current of each pump is 1 mA, and the phase frequency detector gain is $k_P$ = 1 mA/2π radians, or 159 μA/rad. See the Charge Pump (CP) and Phase Detector (PD) section for more information.

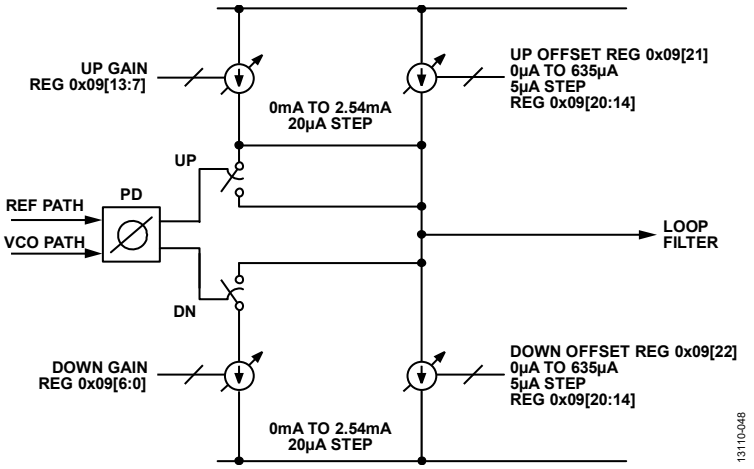



*Figure 26. Charge Pump Gain and Offset Control*

### Charge Pump Phase Offset

In integer mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. Integer mode does not require any CP offset current. When operating in integer mode, disable the CP offset in both directions (up and down) by writing Register 0x09[22:21] = 00b, and set the CP offset magnitude to zero by writing Register 0x09[20:14] = 0.

In fractional mode, CP linearity is of paramount importance. Any nonlinearity degrades phase noise and spurious performance. These nonlinearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always leads, that is, arrives first at the PD).

A programmable CP offset current source adds dc current to the loop filter and creates the desired phase offset. Positive current causes the VCO to lead, whereas negative current causes the reference to lead.

The CP offset is controlled via Register 0x09. Increasing the offset current causes the phase offset to scale from 0° to 360°.

The specific level of charge pump offset current (Register 0x09, Bits[20:14]) is calculated using Equation 9 and shown in Figure 27.

$$Required\ CP\ Offset = min\ ((4.3 \times 10^{-9} \times f_{PD} \times I_{CP}), 0.25 \times I_{CP}) \quad (9)$$

where:
$f_{PD}$ is the comparison frequency of the phase detector (Hz).
$I_{CP}$ is the full-scale current setting (A) of the switching charge pump (set in Register 0x09[6:0] and Register 0x09[13:7]).

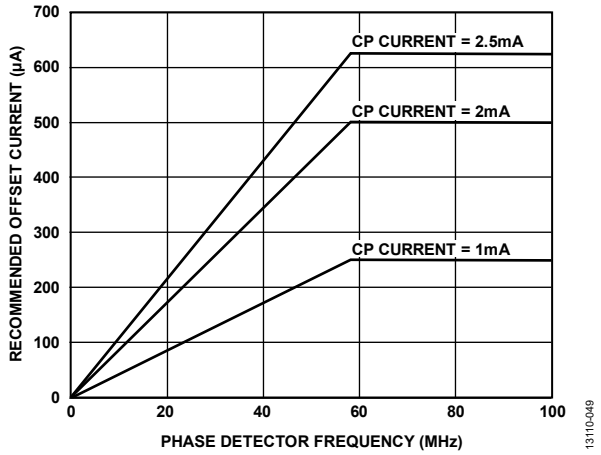



*Figure 27. Recommended CP Offset Current vs. Phase Detector Frequency for Typical CP Gain Currents, Calculated Using Equation 9*

Do not allow the required CP offset current to exceed 25% of the programmed CP current. It is recommended to enable the up offset and disable the down offset by writing Register 0x09[22:21] = 01b.

Operation with CP offset influences the required configuration of the lock detect function. See the description of the lock detect function in the Lock Detect section.

### Phase Detector Functions

Register 0x0B, the phase detector register, provides access to special phase detector features.

Setting Register 0x0B[5] = 0 masks the PD up output, which prevents the charge pump from pumping up.

Setting Register 0x0B[6] = 0 masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Register 0x0B[5] and Register 0x0B[6] tri-states the charge pump while leaving all other functions operating internally.

The PD force CP up (Register 0x0B[9] = 1) and force CP down (Register 0x0B[10] = 1) bits allow the charge pump to be forced up or down, respectively. This forces the VCO to the ends of the tuning range, which is useful in testing the VCO or the continuity of the loop filter path.

### Reference Input Stage

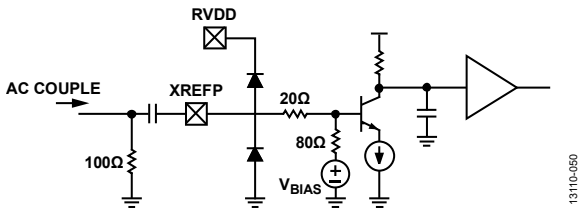



*Figure 28. Reference Path Input Stage*

The reference buffer provides the path from an external reference source (generally crystal-based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Register 0x08[21]. High gain (Register 0x08[21] = 0) is recommended below 200 MHz, and high frequency (Register 0x08[21] = 1) for 200 MHz to 350 MHz operation. The buffer is internally dc biased with 100 Ω internal termination. For a 50 Ω match, add an external 100 Ω resistor to ground followed by an ac coupling capacitor (impedance less than 1 Ω).

At low frequencies, a relatively square reference is recommended to maintain a high input slew rate. At higher frequencies, use a square or sinusoid. Table 8 shows the recommended operating regions for different reference frequencies. If operating outside these regions, the device usually still operates, but with degraded reference path phase noise performance.

When operating at 50 MHz, the input referred phase noise of the PLL is between −148 dBc/Hz and −150 dBc/Hz at a 10 kHz offset, depending on the mode of operation. To avoid degradation of the PLL noise contribution, the input reference signal must be 10 dB better than this floor. Such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

### Reference Path R Divider

The reference path R divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled via Register 0x02.

### RF Path, N Divider

The main RF path divider is capable of average divide ratios between $2^{19}$ – 5 (524,283) and 20 in fractional mode, and between $2^{19}$ – 1 (524,287) and 16 in integer mode. Normally, the VCO frequency range divided by the minimum N divider value can result in practical restrictions on the maximum usable PD frequency. For example, a VCO operating at 1.5 GHz in fractional mode with a minimum N divider value of 20 has a maximum PD frequency of 75 MHz. This isn't the case with the ADF5610 regardless of the mode of operation or the PD frequency. For RFOUT frequencies less than 8GHz the minimum frequency at the input to the PLL will be 3500 MHz so N will always be greater than the minimum regardless of the mode. When RFOUT equals 8.0GHz, the internal prescaler of the PLL (REG 0x08[19]), must be enabled. This results in the 4.0GHz fundamental frequency being divided down such that 2.0GHz will be supplied to the PLL input. Operating in integer mode allows PD rates up to 115MHz. This results in an N value of 17 which isn't a problem. Operation in fractional mode limits the PD rate to 100MHz which results in the minimum value for N when RFOUT equals 8.0 GHz, but no less.

### Lock Detect

The lock detect (LD) function verifies that the ADF5610 is generating the desired frequency. It is enabled by writing Register 0x07[3] = 1. The ADF5610 provides an LD indicator in one of two ways.

- As an output available on the LD/SDO pin of the ADF5610 (configuration is required to use the LD/SDO pin for LD purposes; for more information, see the Serial Port and the Configuring the LD/SDO Pin for LD Output sections).
- Reading from Register 0x12[1], where Bit 1 = 1 indicates a locked condition and Bit 1 = 0 indicates an unlocked condition.

The LD circuit expects the divided VCO edge and the divided reference edge to appear at the PD within a user specified time period (window), repeatedly. Either signal may arrive first. Only the difference in arrival times is significant. The arrival of the two edges within the designated window increments an internal counter. When the count reaches and exceeds a user specified value (Register 0x07[2:0]), the ADF5610 declares lock.

Failure in registering the two edges in any one window resets the counter and immediately declares an unlocked condition. Lock is deemed to be re-established when the counter reaches the user specified value (Register 0x07[2:0]) again.

The ADF5610 supports two lock detect modes.

- Analog LD supports a fixed window size of 10 ns. Analog LD mode is selected by writing Register 0x07[6] = 0.
- Digital LD supports a user configurable window size, programmed in Register 0x07[11:7]. Digital LD is selected by writing Register 0x07[6] = 1.

#### Lock Detect Configuration

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration, described in detail in the Charge Pump (CP) and Phase Detector (PD) section.

The settings in Register 0x09 impact the required LD window size in fractional mode of operation. To function properly, the

required lock detect window size is provided by Equation 10 in fractional mode and Equation 11 in integer mode.

$$LD\ Window\ (\text{sec}) = \frac{\left(\frac{I_{CP\_OFFSET}\ (\text{A})}{f_{PD}(\text{Hz}) \times I_{CP}\ (\text{A})} + \frac{1}{f_{PD}(\text{Hz})}\right)}{2} \quad (10)$$

$$LD\ Window\ (\text{sec}) = \frac{1}{2 \times f_{PD}} \quad (11)$$

where:

$f_{PD}$ is the comparison frequency of the phase detector.

$I_{CP\_OFFSET}$ is the charge pump offset current (Register 0x09[20:14]).

$I_{CP}$ is the full-scale current setting of the switching charge pump (Register 0x09[6:0] or Register 0x09[13:7]).

If the result provided by Equation 10 is equal to 10 ns, analog LD can be used (Register 0x07[6] = 0); otherwise, digital LD is necessary (Register 0x07[6] = 1).

Table 9 lists the required Register 0x07 settings to appropriately program the digital LD window size. From Table 9, select the closest value in the digital LD window size columns to the ones calculated in Equation 10 and Equation 11, and program Register 0x07[11:10] and Register 0x07[9:7] accordingly.

**Table 8. Reference Sensitivity**[1]

| Reference Input Frequency (MHz) | Square Input | | | Sinusoidal Input | | |
|---|---|---|---|---|---|---|
| | Slew > 0.5 V/ns | Recommended Swing (V p-p) | | | Recommended Power Range (dBm) | |
| | Recommended | Minimum | Maximum | Recommended | Minimum | Maximum |
| <10 | Yes | 0.6 | 2.5 | No | No | No |
| 10 | Yes | 0.6 | 2.5 | No | No | No |
| 25 | Yes | 0.6 | 2.5 | Okay | 8 | 15 |
| 50 | Yes | 0.6 | 2.5 | Yes | 6 | 15 |
| 100 | Yes | 0.6 | 2.5 | Yes | 5 | 15 |
| 150 | Okay | 0.9 | 2.5 | Yes | 4 | 12 |
| 200 | Okay | 1.2 | 2.5 | Yes | 3 | 8 |

[1] Okay means the setting works. For example, 150 MHz input square wave is sufficient but 100 MHz may provide improved performance.

### Digital Window Configuration Example

For this example, assume the device is in fractional mode, with a 50 MHz PD and the following conditions:

- Charge pump gain of 2 mA (Register 0x09[13:7] = 0x64, Register 0x09[6:0] = 0x64),
- Up offset (Register 0x09[22:21] = 01b)
- Offset current magnitude of 400 µA (Register 0x09[20:14] = 0x50)

Apply Equation 10 to calculate the required LD window size.

$$LD\ Window\ (\text{sec}) = \frac{\left(\frac{0.4 \times 10^{-3}\ (\text{A})}{50 \times 10^{6}\ (\text{Hz}) \times 2 \times 10^{-3}\ (\text{A})} + 2.66 \times 10^{-9}\ (\text{sec}) + \frac{1}{50 \times 10^{6}\ (\text{Hz})}\right)}{2}$$

$$= 13.33\ \text{ns}$$

Locate the Table 9 value that is closest to this result, which is, in this case, 13.3 ≈ 13.33. To set the digital LD window size, program Register 0x07[11:10] = 10b and Register 0x07[9:7] = 010b, according to Table 9. For a given operating point, there is always a good solution for the lock detect window. However, one solution does not fit all operating points. As observed from Equation 10 and Equation 11, if the charge pump offset or PD frequency is changed significantly, the lock detect window may need to be adjusted.

**Table 9. Typical Digital Lock Detect Window**

| LD Timer Speed, Register 0x07[11:10] | Digital Lock Detect Window Size Nominal Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | LD Timer Divide Setting, Register 0x07[9:7] | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 00 (Fastest) | 6.5 | 8 | 11 | 17 | 29 | 53 | 100 | 195 |
| 01 | 7 | 8.9 | 12.8 | 21 | 36 | 68 | 130 | 255 |
| 10 | 7.1 | 9.2 | 13.3 | 22 | 38 | 72 | 138 | 272 |
| 11 Slowest | 7.6 | 10.2 | 15.4 | 26 | 47 | 88 | 172 | 338 |

### Configuring the LD/SDO Pin for LD Output

Setting Register 0x0F[7] = 1 and Register 0x0F[4:0] = 1 displays the lock detect flag on the LD/SDO pin of the ADF5610. When locked, LD/SDO is high. As the name suggests, the LD/SDO pin is multiplexed between the LD and the serial data output (SDO) signals. Therefore, LD is available on the LD/SDO pin at all times except when a serial port read is requested, in which case the pin reverts temporarily to the serial data output pin, and returns to the lock detect flag after the read is completed.

LD can be made available on the LD/SDO pin at all times by writing Register 0x0F[6] = 1. In that case, the ADF5610 does not provide any readback functionality because the SDO signal is not available.

## *Cycle Slip Prevention (CSP)*

When changing the VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Because the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD cycles from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump cycles from maximum to minimum, even though the VCO has not yet reached its final frequency.

The charge on the loop filter small capacitor may actually discharge slightly during the low gain portion of the cycle. This discharge can make the VCO frequency reverse temporarily during locking. This phenomenon is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle slipping increases the time to lock to a value greater than that predicted by normal small signal Laplace transform analysis.

The ADF5610 PD features an ability to reduce cycle slipping during acquisition. The cycle slip prevention (CSP) feature increases the PD gain during large phase errors. The specific phase error that triggers the momentary increase in PD gain is set via Register 0x0B[8:7].

## *Frequency Tuning*

The ADF5610 VCO subsystem always operates in the doubled frequency range of operation (7000 MHz to 15000 MHz) which is always available at the RFOUT port or at the differential divider ports, PDIVOUT and NDIVOUT when the divider is set to divide-by-1 in VCO_REG 0x02[2:0].

Frequencies at or below its fundamental frequency of operation (55 MHz to 7000 MHz) are realized by tuning to the appropriate doubled frequency and selecting the appropriate output divider setting (divide by 2 to 128) in VCO_REG 0x02[2:0].

The fundamental band of operation (3500 MHz to 7500 MHz) is input to the internal PLL and is not directly available to the user. For more information, see the VCO Autocalibration section.

### Integer Mode

The ADF5610 is capable of operating in integer mode. For integer mode, set the following registers:

- Disable the fractional modulator, Register 0x06[11] = 0
- Bypass the modulator circuit, Register 0x06[7] = 1

In integer mode, the VCO step size is fixed to that of the PD frequency. Integer mode typically has a 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used; therefore, lower phase noise can often be realized in fractional mode. Disable the charge pump offset when in integer mode.

### Integer Frequency Tuning

In integer mode, the digital Σ-Δ modulator is shut off and the N divider (Register 0x03) can be programmed to any integer value in the range of 16 to $2^{19} - 1$. To run in integer mode, configure Register 0x06 (as described above in the Configuring the LD/SDO Pin for LD Output section), then program the integer portion of the frequency as explained by Equation 12, ignoring the fractional part.

1. Disable the fractional modulator, Register 0x06[11] = 0.
2. Bypass the Σ-Δ modulator Register 0x06[7] = 1.
3. Since the fundamental frequency (3500 MHz – 7500 MHz) range is supplied to the PLL this will the basis for all programming.
4. If the fundamental frequency is <4000MHz (RFOUT < 8000MHz), set the internal prescaler, to divide-by-1 (REG 0x08[19] = 0), otherwise set it to 1.
5. To tune to frequencies (<7000 MHz), select the appropriate output divider value VCO_REG 0x02[2:0] then enable the differential output divider VCO_REG 0x01[8].

Writing to the VCO subsystem registers (VCO_REG 0x02[2:0] and VCO_REG 0x01[8] in this case) is accomplished indirectly through PLL Register 0x05. More information on communicating with the VCO subsystem through PLL Register 0x05 is available in the VCO Serial Port Interface (VSPI) section.

### Fractional Mode

Set the following registers to place the ADF5610 in fractional mode:

- Enable the fractional modulator, Register 0x06[11] = 1.
- Connect the Σ-Δ modulator in circuit, Register 0x06[7] = 0.

**Fractional Frequency Tuning**

This is a generic example with the goal of explaining how to program the output frequency. Actual variables are dependent on the reference in use.

The ADF5610 in fractional mode achieves frequencies at fractional multiples of the reference. The frequency of the ADF5610 is given by

$$f_{RF} = 2 \times f_{VCO}$$

where:

$$f_{VCO} = \frac{f_{XTAL}}{R}(N_{INT} + N_{FRAC}) = f_{INT} + f_{FRAC} \quad (12)$$

and $f_{div} = f_{RF} / k$ (13)

where:

$f_{RF}$ is the doubled frequency (RFOUT)

$f_{VCO}$ is the fundamental frequency (input to PLL) after any necessary correction, $f_{VCO}$ must always be less than or equal to 4000MHz. When $f_{VCO}$ is greater than or equal to 400MHz the internal divide-by-2 prescaler (REG 0x08[19]) must be enabled.
$f_{DIV}$ is the output frequency after any potential dividers.
$k$ is 1 for fundamental, or $k$ = 2 to 128 depending on the selected output divider value (Register 0x05[8:0] indirectly addressed to VCO_REG 0x02[2:0]).
$N_{INT}$ is the integer division ratio (set in Register 0x03), an integer number between 20 and 524,284.
$N_{FRAC}$ is the fractional part, from 0.0 to 0.99999…, $N_{FRAC}$ = Register 0x04/$2^{24}$.
$R$ is the reference path division ratio (set in Register 0x02).
$f_{XTAL}$ is the frequency of the reference oscillator input.

For example, $f_{DIV}$ = 1752.5 MHz, k = 2, $f_{VCO}$ = 3505 MHz, $f_{RF}$ = 7010 MHz, $f_{XTAL}$ = 50 MHz, R = 1, $f_{PD}$ = 50 MHz, $N_{INT}$ = 70, and $N_{FRAC}$ = 0.1. $f_{PD}$ is the PD operating frequency, $f_{XTAL}$/R.

Register 0x04 = round(0.1 × $2^{24}$) = round(1,677,721.6) = 1,677,722.

If $f_{VCO} \geq$ 4000MHz then REG 0x08[19] = 0 (divide-by-1), (14)

else REG 0x08[19] = 1 (divide-by-2)

$f_{VCO}$ (50 × $10^6$ / 1) (70 + 1677722 / $2^{24}$) = 3505 MHz + (15)

1.192 Hz error

$$f_{RF} = 2 \times f_{VCO} = 7010 \text{ MHz} + 2.384 \text{ Hz error} \quad (16)$$

$$f_{DIV} = f_{RF} / k = 3505 \text{ MHz} + 1.192 \text{ Hz error} \quad (17)$$

In this example, the differential divider output frequency of 1752.5 MHz is achieved by programming the 19-bit binary value of 70d = 0x46 into the INTG_REG bit in Register 0x03, and the 24-bit binary value of 1677722d = 0x19999A into the FRAC bit in Register 0x04. Eliminate the 0.596 Hz quantization error using the exact frequency mode, if required. In this example, the output fundamental is divided by 2. Specific control of the output divider is required. See the VCO Subsystem Register Map section and description for details.

**Exact Frequency Tuning**

Due to quantization effects, the absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example, the frequency resolution of a 24-bit fractional modulator is set by the PD comparison rate divided by $2^{24}$. The $2^{24}$ value in the denominator is sometimes referred to as the modulus. Analog Devices PLLs use a fixed modulus, which is a binary number. In some types of fractional PLLs, the modulus is variable, allowing exact frequency steps to be achieved with decimal step sizes. Unfortunately, small steps using small modulus values result in large spurious outputs at multiples of the modulus period (channel step size). For this reason, Analog Devices PLLs use a large fixed modulus. Normally, the step size is set by the size of the fixed modulus. In the case of a 50 MHz PD rate, a modulus of $2^{24}$ results in a 2.98 Hz step resolution, or 0.0596 ppm. In some applications, it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (for example, N = 50.0, 50.5, 50.25, 50.75, …). Some common frequencies cannot be exactly represented. For example, $N_{FRAC}$ = 0.1 = 1/10 must be approximated as round((0.1 × $2^{24}$)/$2^{24}$ ) ≈ 0.100000024. At $f_{PD}$ = 50 MHz, this translates to a 1.2 Hz error. The exact frequency mode of the ADF5610 addresses this issue and can eliminate quantization error by programming the channel step size to $f_{PD}$/10 in Register 0x0C to 10 (in this example). More generally, this feature can be used whenever the desired frequency, $f_{VCO}$, can be exactly represented on a step plan where there is an integer number of steps (<$2^{14}$) across integer-N boundaries. Mathematically, this situation is satisfied if

$$f_{VCOk} \bmod(f_{GCD}) = 0 \quad (16)$$

where:

$f_{VCOk}$ is the channel step frequency. $0 < k < 2^{24} - 1$, as shown in Figure 29.

*GCD* is the greatest common divisor.

$$f_{GCD} = GCD(f_{VCO1}, f_{PD}) \text{ and } f_{GCD} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

where $f_{PD}$ is the frequency of the phase detector.

Some fractional PLLs are able to achieve these exact frequencies by adjusting (shortening) the length of the phase accumulator (the denominator or the modulus of the Σ-Δ modulator) so that the Σ-Δ modulator phase accumulator repeats at an exact period related to the interval frequency ($f_{VCOk} - f_{VCO(k-1)}$) in Figure 29. Consequently, the shortened accumulator results in more frequent repeating patterns and, as a result, often leads to spurious emissions at multiples of the repeating pattern period, or at harmonic frequencies of $f_{VCOk} - f_{VCO(k-1)}$. For example, in some applications, these intervals may represent the spacing between radio channels, with the spurious occurring at multiples of the channel spacing.

In comparison, the Analog Devices method is able to generate exact frequencies between adjacent integer-N boundaries while still using the full 24-bit phase accumulator modulus, thus achieving exact frequency steps with a high phase detector comparison rate, which allows Analog Devices PLLs to maintain excellent phase noise and spurious performance in the exact frequency mode.

**Using Exact Frequency Mode**

If the constraint in Equation 16 is satisfied, the ADF5610 is able to generate signals with zero frequency error at the desired VCO frequency. Exact frequency mode can be reconfigured for each target frequency or be set up for a fixed $f_{GCD}$ that applies to all channels.

**Configuring Exact Frequency Mode for a Particular Frequency**

1) Calculate and program the integer register setting.

$$Register\ 0x03 = N_{INT} = \text{floor}(f_{VCO}/f_{PD})$$

where the floor function is the rounding down to the nearest integer.

2) Then calculate the integer boundary frequency.

$$f_N = N_{INT} \times f_{PD}$$

Calculate and program the exact frequency register value.

$$Register\ 0x0C = f_{PD}/f_{GCD}$$

where $f_{GCD} = GCD(f_{VCO}, f_{PD})$.

Calculate and program the fractional register setting.

$$Register\ 0x04\ N_{FRAC} = \text{ceil}\left(\frac{2^{24}(f_{VCOk} - f_N)}{f_{PD}}\right)$$

where ceil is the ceiling function, that is, round up to the nearest integer.

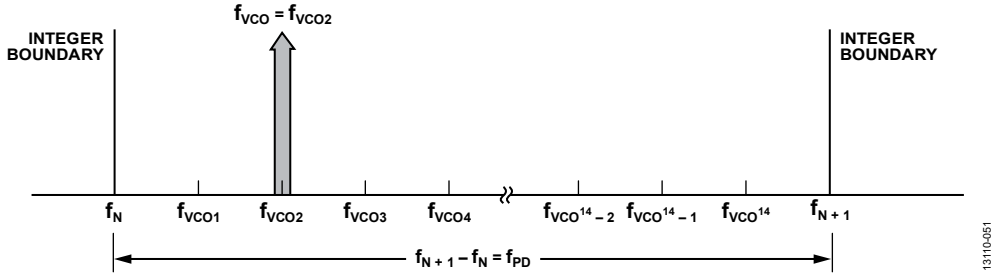



*Figure 29. Exact Frequency Tuning*

(17)

### *Seed Register*

The start phase of the fractional modulator digital phase accumulator (DPA) can be set to one of four possible default values via the seed bits, Register 0x06[1:0]. The ADF5610 automatically reloads the start phase (seed value) into the DPA every time a new fractional frequency is selected. Certain zero or binary seed values may cause spurious energy correlation at specific frequencies. For most cases, a random (not zero and not binary) start seed is recommended (Register 0x06[1:0] = 2).

## SOFT RESET AND POWER-ON RESET

The ADF5610 features a hardware power-on reset (POR). All chip registers are reset to default states approximately 250 µs after power-up.

The PLL subsystem SPI registers can also be soft reset by an SPI write to Register 0x00. Note that the soft reset does not clear the SPI mode of operation referred to in the Serial Port section. The VCO subsystem is not affected by the PLL soft reset; the VCO

subsystem registers can only be reset by removing the power supply.

If external power supplies or regulators have rise times slower than 250 µs, write to the SPI soft reset bit (Register 0x00[5] = 1) immediately after power-up, before any other SPI activity. This write procedure ensures starting from a known state.

## POWER-DOWN MODE

The VCO subsystem is not affected by the CEN pin or soft reset. Therefore, device power-down is a two-step process.

1. Power down the VCO by writing 1 to VCO_REG 0x02[3] Register 2 via Register 0x05.
2. Power-down the PLL by pulling the CEN pin (Pin 17) low (assuming there are no SPI overrides (Register 0x01[0] = 1)). Pulling the CEN pin low disables all analog functions and internal clocks. Current consumption typically drops below 10 µA in the power-down state. The serial port still responds to normal communication in power-down mode.

It is possible to ignore the CEN pin by setting Register 0x01[0] = 0. Control of the power-down mode then comes from the serial port register, Register 0x01[1].

It is also possible to leave various blocks turned on when in power-down (see Register 0x01), as listed in Table 10.

**Table 10. Bit and Block Assignments for Register 0x01**

| Bit Assignment | Block Assignment |
|---|---|
| Bit 2 | Internal bias reference sources |
| Bit 3 | PD block |
| Bit 4 | CP block |
| Bit 5 | Reference path buffer |
| Bit 6 | VCO path buffer |
| Bit 7 | Digital I/O test pads |

## GENERAL-PURPOSE OUTPUT (GPO)

The PLL shares the LD/SDO (lock detect/serial data output) pin to perform various functions. Although the pin is most commonly used to read back registers from the chip via the SPI, it is also capable of exporting a variety of signals and real-time test waveforms (including lock detect). It is driven by a tri-state CMOS driver with ~200 Ω $R_{OUT}$. It has logic associated with it to dynamically select whether the driver is enabled, and to decide which data to export from the chip.

In its default configuration, after power-on reset, the output driver is disabled, and drives only during appropriately addressed SPI reads. This configuration allows the ADF5610 to share its output with other devices on the same bus.

The pin driver is enabled if the chip is addressed; that is, the last three bits of the SPI cycle = 000b before the rising edge of SEN. If SEN rises before SCK has clocked in an invalid (nonzero) chip address, the ADF5610 starts to drive the bus.

To monitor any of the GPO signals, including lock detect, set Register 0x0F[7] = 1 to keep the SDO driver always on. This setting stops the LDO driver from tri-stating and means that the SDO line cannot be shared with other devices.

The ADF5610 naturally switches from the GPO data and exports the SDO signal during an SPI read. To prevent this automatic data selection and always select the GPO signal, set Bit 6 of Register 0x0F to 1 to prevent auto-muxing of the LD/SDO pin. The phase noise performance at this output is poor and uncharacterized. Also, do not toggle the GPO output during normal operation because toggling may degrade the spectral performance.

Additional controls are available that may be helpful when sharing the bus with other devices.

- To disable the driver completely, set Register 0x08[5] = 0 (this bit takes precedence over all other LD/SDO driver bit settings).
- To disable either the pull-up or pull-down sections of the driver, set Register 0x0F[8] = 1 or Register 0x0F[9] = 1, respectively.
- To drive 3.3 V CMOS logic, set Register 0x0B[22] = 1.

Example scenarios are listed in Table 11. The signals that are available on the GPO are selected by changing the GPO_SELECT bits, Register 0x0F[4:0].

## CHIP IDENTIFICATION

Identify the PLL subsystem version information by reading the content of the read only register, CHIP_ID, in Register 0x00. It is not possible to read the VCO subsystem version.

## SERIAL PORT INTERFACE (SPI)

The ADF5610 SPI supports both 1.8 V and 3.3 V input voltage levels. Input pins including SDI, SCK, and SEN support both voltage levels without the need for any configuration.

The SPI output, (LD/SDO pin), only supports 3.3 V levels when driven and 1.8 V / 3.3 in open drain mode.
The configuration (CMOS or open drain) is register programmable via Register 0x0F[9:8]. Open-drain mode requires an external pull-up resistor. See the electrical specifications in Table 1 for more information.

### *SPI Protocol Features*

The SPI protocol has the following general features:

- 3-bit chip address, can address up to eight devices connected to the serial bus.
- Wide compatibility with multiple protocols from multiple vendors.
- Simultaneous write/read during the SPI cycle.

- 5-bit address space.
- 3-wire for write only capability, 4-wire for read/write capability.

Typical serial port operation can be run with SCK at speeds of up to 50 MHz.

### *Serial Port Write Operation*

SPI write specifications are listed in Table 2 in the SPI Write Timing Characteristics section and a typical write cycle is shown in Figure 30. The SPI write operation is as follows:

1. The master (host) places 24-bit data, D[23:0], MSB first, on SDI on the first 24 falling edges of SCK.
2) The slave (ADF5610) shifts in data on SDI on the first 24 rising edges of SCK.

The master places a 5-bit register address to be written to, R[4:0], MSB first, on the next five falling edges of SCK (25th to 29th falling edges).
The slave shifts the register bits on the next five rising edges of SCK (25th to 29th rising edges).
The master places a 3-bit chip address, A[2:0], MSB first, on the next three falling edges of SCK (30th to 32nd falling edges).
Analog Devices reserves Chip Address A2 to Chip Address A0 = 000 for all RF PLLs with integrated VCOs.
The slave shifts the chip address bits on the next three rising edges of SCK (30th to 32nd rising edges).
The master asserts SEN after the 32nd rising edge of SCK.
The slave registers the SDI data on the rising edge of SEN.

**Table 11. Driver Scenarios**

| Scenario | Action |
|---|---|
| Drive SDO During Reads, Lock Detect Otherwise | Set GPO select, Register 0x0F[4:0] = 00001b (default)<br>Set Register 0x0F[6] = 0, enable automux of SDO<br>Set Register 0x0F[7] = 1, prevent GPO driver disable |
| Always Drive Lock Detect, 3.3 V Output | Set Register 0x0F[6] = 1, prevent automux of SDO<br>Set the GPO select, Register 0x0F[4:0] = 00001 (default)<br>Set Register 0x0F[7] = 1, prevent GPO driver disable |

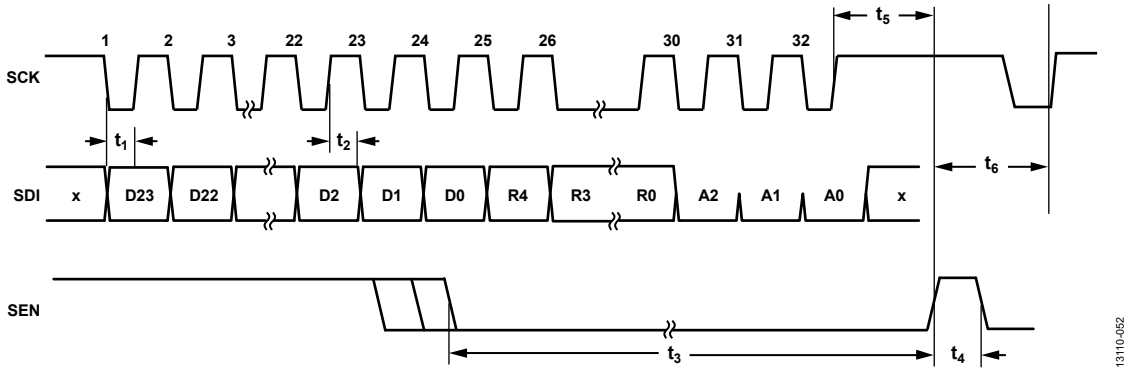



*Figure 30. Serial Port Write Timing Diagram*

### *Serial Port Read Operation*

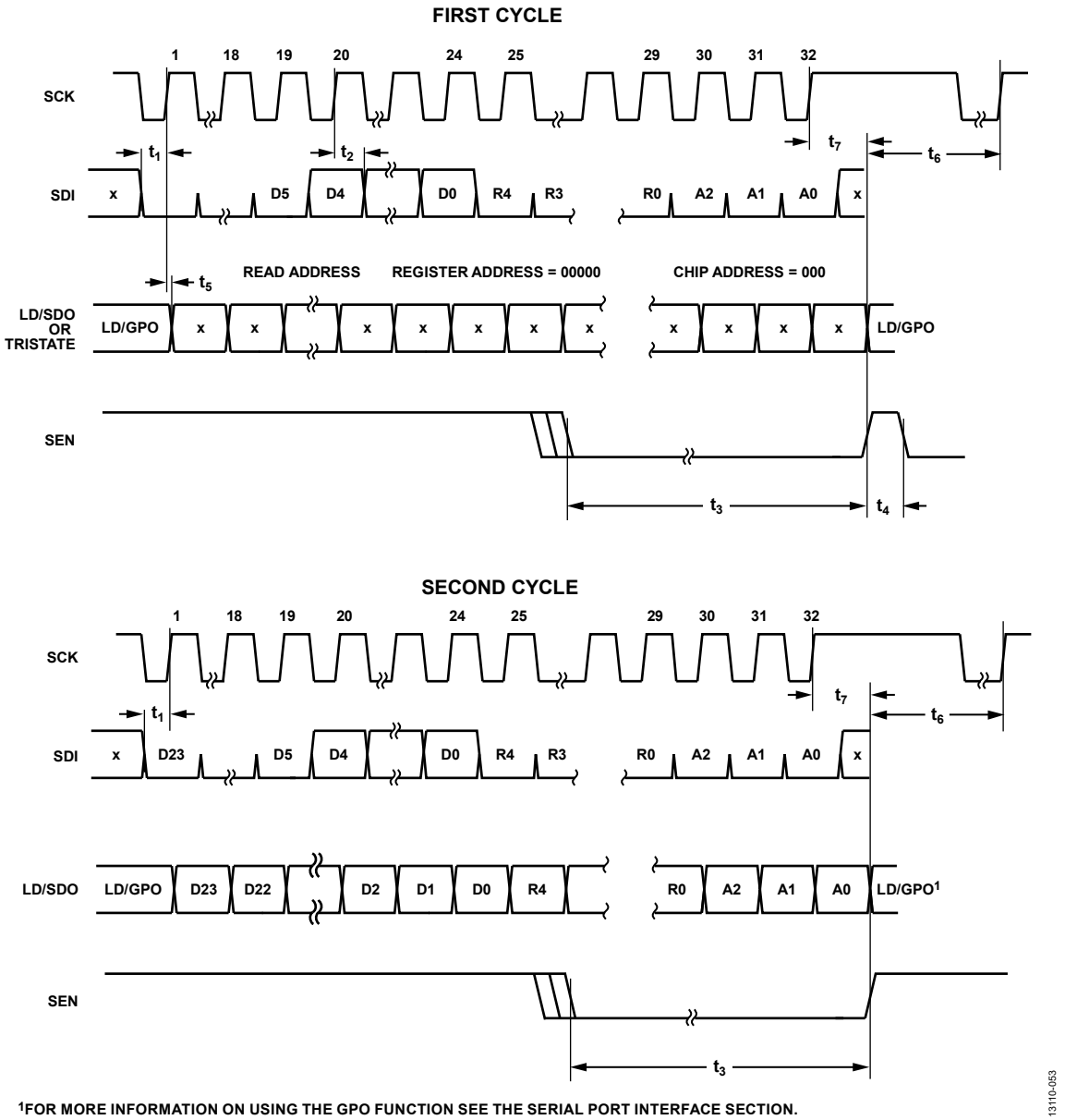
In general, the LD/SDO line is always active during the write cycle. During any SPI cycle, LD/SDO contains the data from the current address written in Register 0x00[4:0]. If Register 0x00[4:0] is not changed, the same data is always present on LD/SDO during a SPI cycle.

If a read is required from a specific address, it is necessary to write the required address to Register 0x00[4:0] in the first SPI cycle. Then, in the next SPI cycle, the desired data becomes available on LD/SDO. A typical read cycle is shown in Figure 31.

An example of the two-cycle procedure to read from any random address is as follows:

1. The master (host), on the first 24 falling edges of SCK, places 24-bit data, D[23:0], MSB first, on SDI, as shown in Figure 31. Set D[23:5] to zero. D[4:0] = address of the register to be read on the next cycle.
2. The slave (ADF5610) shifts in data on SDI on the first 24 rising edges of SCK.
3. The master places the 5-bit register address, R[4:0] (the read address register), MSB first, on the next five falling edges of SCK (25th to 29th falling edges). R[4:0] = 00000.
4. The slave shifts the register bits on the next five rising edges of SCK (25th to 29th rising edges).
5. The master places the 3-bit chip address, A[2:0], MSB first, on the next three falling edges of SCK (30th to 32nd falling edges). The chip address is always 000b.

6. The slave shifts the chip address bits on the next three rising edges of SCK (30th to 32nd rising edges).
7. The master asserts SEN after the 32nd rising edge of SCK.
8. The slave registers the SDI data on the rising edge of SEN.
9. The master clears SEN to complete the address transfer of the two-part read cycle.
10. If a write data to the chip is not needed at the same time as the second cycle occurs, it is recommended to simply rewrite the same contents on SDI to Register 0x00 on the readback portion of the cycle.
11. The master places the same SDI data as the previous cycle on the next 32 falling edges of SCK.
12. The slave (ADF5610) shifts the SDI data on the next 32 rising edges of SCK.
13. The slave places the desired read data (that is, data from the address specified in Register 0x00[4:0] of the first cycle) on LD/SDO, which automatically switches to SDO mode from LD mode, disabling the LD output.
14. The master asserts SEN after the 32nd rising edge of SCK to complete the cycle and to revert back to lock detect on LD/SDO.




[1]FOR MORE INFORMATION ON USING THE GPO FUNCTION SEE THE SERIAL PORT INTERFACE SECTION.

*Figure 31. Serial Port Read Timing Diagram*

## POWER SUPPLY

The ADF5610 is a high performance, low noise device. Phase noise and spurious performance may be degraded by noisy power supplies. To achieve maximum performance and ensure that power supply noise does not degrade the performance of the ADF5610, it is recommended to use Analog Devices low noise, high power supply rejection ratio (PSRR) regulators. Preferred regulators include the LT3042, LT3045, ADM7150 or ADM7151. Good performance and supply isolation may also be achievable with the HMC1060LP3E quad low noise regulator.

## PROGRAMMABLE PERFORMANCE TECHNOLOGY

For low power applications that do not require maximum noise floor performance, the ADF5610 features the ability to reduce current consumption by 18 mA (power consumption by 90 mW)

High performance is enabled by writing VCO_REG 0x01[4:2] = 7d, and it is disabled (low current consumption mode enabled) by writing VCO_REG 0x01[4:2] = 0d. High performance mode improves noise floor performance at the cost of increased current consumption.

## LOOP FILTER AND FREQUENCY CHANGES

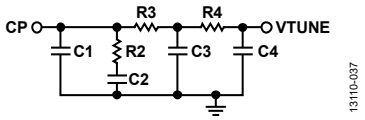



*Figure 32. Loop Filter Design*

All PLLs with integrated VCOs exhibit integer boundary spurs at harmonics of the reference frequency. Figure 18 shows the worst case spurious scenario where the harmonic of the reference frequency (50 MHz) is within the loop filter bandwidth of the fundamental frequency of the ADF5610.

A tunable reference could be employed to vary the reference frequency and to distance the harmonic of the reference frequency (spurious emissions) from the fundamental output frequency of the ADF5610 so that it is filtered by the loop filter. The internal ADF5610 setup and divide ratios would be changed in the opposite direction accordingly so that the ADF5610 generates an identical output frequency without the spurious emissions inside the loop bandwidth. Using these same procedures.

The ADF5610 features an internal autocalibration process that seamlessly calibrates the ADF5610 when a frequency change is executed. When the ADF5610 is calibrated at any temperature, the calibration setting is guaranteed to hold across the entire operating range of the ADF5610 (−40°C to +85°C). The tuning voltage is maintained within a narrow operating range for worst case scenarios where calibration is executed at one temperature extreme and the device is operating at the other extreme.

For applications that require fast frequency changes, the ADF5610 supports manual calibration that enables faster settling times. Manual calibration must be executed only once for each individual ADF5610 device, at any temperature, and is valid across all temperature operating ranges of the ADF5610. For more information about manual calibration, see the Manual VCO Calibration for Fast Frequency Hopping section. Any size frequency hop has a similar settling time with autocalibration disabled (Register 0x0A[11] = 1).

## MUTE MODE

The ADF5610 has some to support muting of the outputs. The differential divider outputs PDIVOUT and NDIVOUT can be disabled be setting VCO_REG 0x01[8] = 0 to power down the divider when not in use. The RFOUT port can only be muted by powering down the VCO from VCO_REG 0x02[3] however this also effectively mutes the differential divider outputs simultaneously as no signal will be present at the input of the buffer to the divider.

# PLL REGISTER MAP

## ID, READ ADDRESS, AND RESET (RST) REGISTERS

The ID register is read only, the read address/RST strobe register is write only, and the RST register is read/write.

**Table 12. Register 0x00, ID Register (Read Only)**

| Bits | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 23:0 | R | CHIP_ID | 24 | A7975 | ADF5610 chip ID |

**Table 13. Register 0x00, Read Address/RST Strobe Register (Write Only)**

| Bits | Type | Name | Width | Default[1] | Description |
|---|---|---|---|---|---|
| 4:0 | W | Read address | 5 | N/A | Read address for next cycle when in Open Mode, 2 cycle read. This is a write only register. |
| 5 | W | Soft reset | 1 | N/A | Soft reset for both SPI modes (set to 0 for proper operation). Resets all registers to defaults. |
| 23:6 | W | Not defined | 18 | N/A | Not defined (set to 0 for proper operation). |

[1] N/A means not applicable.

**Table 14. Register 0x01, RST Register (Default 0x000002)**

| Bits | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 0 | R/W | RST_CHIPEN_PIN_SELECT | 1 | 0 | 1 = power down the PLL via the CEN pin (see the Power-Down Mode section)<br>0 = power down the PLL via the SPI (RST_CHIPEN_FROM_SPI), Register 0x01[1] |
| 1 | R/W | RST_CHIPEN_FROM_SPI | 1 | 1 | PLL enable bit of the SPI |
| 2 | R/W | KEEP_BIAS_ON | 1 | 0 | Keeps internal bias generators on, ignores chip enable control |
| 3 | R/W | KEEP_PFD_ON | 1 | 0 | Keeps PFD circuit on, ignores chip enable control |
| 4 | R/W | KEEP_CP_ON | 1 | 0 | Keeps charge pump on, ignores chip enable control |
| 5 | R/W | KEEP_REF_BUF_ON | 1 | 0 | Keeps reference buffer block on, ignores chip enable control |
| 6 | R/W | KEEP_VCO_ON | 1 | 0 | Keeps VCO divider buffer block on, ignores chip enable control |
| 7 | R/W | KEEP_GPO_DRIVER_ON | 1 | 0 | Keeps GPO output driver on, ignores chip enable control |
| 8 | R/W | Reserved | 1 | 0 | Reserved. Program 0 |
| 9 | R/W | Reserved | 1 | 0 | Reserved. Program 0 |

## REFERENCE DIVIDER (REFDIV), INTEGER, AND FRACTIONAL FREQUENCY REGISTERS

**Table 15. Register 0x02, REFDIV Register (Default 0x000001)**

| Bits | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 13:0 | R/W | RDIV | 14 | 1 | Reference divider R value (see Equation 12). Using the divider requires the reference path buffer to be enabled (Register 0x08[3] = 1). 1d ≤ RDIV ≤ 16,383d. |

**Table 16. Register 0x03, Frequency Register, Integer Part (Default 0x000019)**

| Bits | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 18:0 | R/W | INTG_REG | 19 | 25d | Integer divider register. These bits are the VCO divider integer part, used in all modes (see Equation 12).<br>Fractional mode.<br>Min = 0x14 = 20d.<br>Maximum $2^{19} - 4$ = 0x7FFFC = 524,284d.<br>Integer mode.<br>Minimum = 0x10 = 16d. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Maximum $2^{19}$– 1 = 0x7FFFF = 524,287d. |

**Table 17. Register 0x04, Frequency Register, Fractional Part (Default 0x000000)**

| Bits | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 23:0 | R/W | FRAC | 24 | 0 | VCO divider fractional part (24-bit unsigned); see the Fractional Frequency Tuning section. These bits are used in fractional mode only ($N_{FRAC}$ = Register 0x04/$2^{24}$). Minimum = 0d; maximum = $2^{24}$ – 1. |

## VCO SPI REGISTER

Register 0x05 is a special register used for indirect addressing of the VCO subsystem. Writes to Register 0x05 are automatically forwarded to the VCO subsystem by the VCO SPI state machine controller.

The auxiliary SPI (AuxSPI) outputs the contents of "Reg 05h" upon receipt of a frequency change command. The AuxSPI data is output at the AuxSPI clock rate which is based on the fpd rate ("Reg 05h"[6]). A single AuxsPI transfer requires 16 AuxSPI cycles plus 4 overhead cycles.

Register 0x05 is a read/write register. However, Register 0x05 holds only the contents of the last transfer to the VCO subsystem. Therefore, it is not possible to read the full contents of the VCO subsystem. Only the content of the last transfer to the VCO subsystem can be read. For autocalibration, Register 0x05[6:0] must be set to 0.

**Table 18. Register 0x05, VCO SPI Register (Default 0x000000)**

| Bits | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 2:0 | R/W | VCO_ID | 3 | 0 | Internal VCO subsystem ID. |
| 6:3 | R/W | VCO_REGADDR | 4 | 0 | VCO subsystem register address. These bits are for interfacing with the VCO. See the VCO Serial Port Interface (VSPI) section. |
| 15:7 | R/W | VCO_DATA | 9 | 0 | VCO subsystem data. These bits are used to write the data to the VCO subsystem. |

## Σ-Δ CONFIGURATION REGISTER

**Table 19. Register 0x06, Σ-Δ Configuration Register (Default 0x200B4A)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 1:0 | R/W | Seed | 2 | 2 | Selects the seed in fractional mode. Writes to this register are stored in the ADF5610 and are loaded into the modulator only when a frequency change is executed and when Register 0x06[8] = 1.<br>0: 0 seed.<br>1: LSB seed.<br>2: 0xB29D08 seed.<br>3: 0x50F1CD seed. |
| 6:2 | R/W | Reserved | 5 | 18d (0x12) | Reserved. |
| 7 | R/W | FRAC_BYPASS | 1 | 0 | Bypass fractional mode. When bypassing the fractional modulator, the output is ignored, but the fractional modulator continues to be clocked when SD enable = 1. Use this bit to test the isolation of the digital fractional modulator from the VCO output in integer mode.<br>0: use modulator, required for fractional mode<br>1: bypass modulator, required for integer mode. |
| 10:8 | R/W | Initialization | 3 | 3d | Program to 7d. |
| 11 | R/W | SD enable | 1 | 1 | This bit controls whether autocalibration starts on an integer or a fractional write.<br>0: disables fractional core, use for integer mode or integer mode with CSP.<br>1: enables fractional core (required for fractional mode), or integer isolation testing. |
| 20:12 | R/W | Reserved | 9 | 0 | Reserved. |

| | | | | | |
|---|---|---|---|---|---|
| 21 | R/W | Automatic clock configuration | 1 | 1 | Program to 0. |
| 22 | R/W | Reserved | 1 | 0 | Reserved. |

## LOCK DETECT REGISTER

**Table 20. Register 0x07, Lock Detect Register (Default 0x00014D)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 2:0 | R/W | LKD_WINCNT_MAX | 3 | 5d | The lock detect window sets the number of consecutive counts of the divided VCO that must be within the lock detect window to declare lock<br>0: 5<br>1: 32<br>2: 96<br>3: 256<br>4: 512<br>5: 2048<br>6: 8192<br>7: 65,535 |
| 3 | R/W | Enable internal lock detect | 1 | 1 | See the Serial Port section |
| 5:4 | R/W | Reserved | 2 | 0 | Reserved |
| 6 | R/W | Lock detect window type | 1 | 1 | Lock detection window timer selection<br>1: digital programmable timer<br>0: analog one shot, nominal 10 ns window |
| 9:7 | R/W | LD digital window duration | 3 | 2 | Lock detection, digital window duration<br>0: half cycle<br>1: one cycle<br>2: two cycles<br>3: four cycles<br>4: eight cycles<br>5: 16 cycles<br>6: 32 cycles<br>7: 64 cycles |
| 11:10 | R/W | LD digital timer frequency control | 2 | 0 | Lock detect digital timer frequency control (see the Lock Detect section for more information)<br>00: fastest<br>11: slowest |
| 12 | R/W | Reserved | 31 | 0 | Reserved |
| 13 | R/W | Automatic relock: one try | 1 | 0 | 1: attempts to relock if the lock detect fails for any reason; tries one time only. |

## ANALOG ENABLE (EN) REGISTER

**Table 21. Register 0x08, Analog EN Register (Default 0xC1BEFF)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 0 | R/W | BIAS_EN | 1 | 1 | Enables main chip bias reference |
| 1 | R/W | CP_EN | 1 | 1 | Charge pump enable |
| 2 | R/W | PD_EN | 1 | 1 | PD enable |
| 3 | R/W | REFBUF_EN | 1 | 1 | Reference path buffer enable |
| 4 | R/W | VCOBUF_EN | 1 | 1 | VCO path RF buffer enable |
| 5 | R/W | GPO_PAD_EN | 1 | 1 | 0: disables the LD/SDO pin<br>1: enables the GPO port or allows a shared SPI<br>When Bit 5 = 1 and Register 0xF[7] = 1, the LD/SDO pin is always driven, which is required for use of the GPO port<br>When Bit 5 = 1 and Register 0xF[7] = 0, SDO is off, when an unmatched chip address is seen on the SPI, allows shared SPI with other compatible devices |

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 9:6 | R/W | Reserved | 4 | 11d (0x0B) | Reserved Combined separate values shown on 704, using defaults – ok. |
| 10 | R/W | VCO buffer and prescaler bias enable | 1 | 1 | VCO buffer and prescaler bias enable |
| 18:11 | R/W | Reserved | 1 | 55d (0x37) | Program to 55d (0x37). |
| | | | | | |
| | | | | | |
| 19 | R/W | 8 GHz Divide-by-2 En | 1 | 0 | Allows PLL operation up to 8GHz.<br>When input to PLL is less than 4000 MHz set to 0d to bypass internal divider.<br>When input to PLL is greater than or equal to 4.0 GHz set to 1d to enable internal fixed divide-by-2. |
| 20 | R/W | Reserved | 1 | 0 | Program 0. |
| 21 | R/W | High frequency reference | 1 | 0 | Program to 1 for 200 MHz to 350 MHz operation; program to 0 for <200 MHz. |
| 23:22 | R/W | Reserved | 2 | 3d | Reserved Combined separate values shown on 704, using defaults – ok. |

## CHARGE PUMP REGISTER

**Table 22. Register 0x09, Charge Pump Register (Default 0x403264)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 6:0 | R/W | CP down gain | 7 | 100d, 0x64 | Charge pump down gain control, 20 µA per step. Affects fractional phase noise and lock detect settings.<br>0d = 0 µA.<br><br>1d = 20 µA.<br>2d = 40 µA.<br>…<br>127d = 2.54 mA. |
| 13:7 | R/W | CP up gain | 7 | 100d, 0x64 | Charge pump up gain control, 20 µA per step. Affects fractional phase noise and lock detect settings.<br><br>0d = 0 µA.<br>1d = 20 µA.<br>2d = 40 µA.<br>…<br>127d = 2.54 mA. |
| 20:14 | R/W | Offset magnitude | 7 | 0 | Charge pump offset control, 5 µA per step. Affects fractional phase noise and lock detect settings.<br>0d = 0 µA.<br>1d = 5 µA.<br>2d = 10 µA.<br>…<br>127d = 635 µA. |
| 21 | R/W | Offset up enable | 1 | 0 | Recommended setting = 0. |
| 22 | R/W | Offset down enable | 1 | 1 | Recommended setting = 1 in fractional mode, 0 otherwise. |
| 23 | R/W | Reserved | 1 | 0 | Reserved. |

## AUTOCALIBRATION REGISTER

**Table 23. Register 0x0A, VCO Autocalibration Configuration Register (Default 0x002205) – Program to 0x002047**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 2:0 | R/W | VTUNE resolution | 3 | 5 | R divider cycles<br>0: 1 cycle<br>1: 2 cycles<br>2: 4 cycles<br>…<br>7: 256 cycles |
| 9:3 | R/W | Reserved | 7 | 64d | Program 8d |
| 10 | R/W | Force curve | 1 | 0 | Program 0 |
| 11 | R/W | Autocalibration disable | 1 | 0 | Program 0 for normal operation using VCO autocalibration |
| 12 | R/W | No VSPI trigger | 1 | 0 | 0: normal operation<br>1: this bit disables the serial transfers to the VCO subsystem (via Register 0x05) |
| 14:13 | R/W | FSM/VSPI clock select | 2 | 1 | These bits set the autocalibration FSM and VSPI clock (50 MHz maximum)<br>0: input crystal reference<br>1: input crystal reference divide by 4<br>2: input crystal reference divide by 16<br>3: input crystal reference divide by 32 |
| 16:15 | R/W | Reserved | 2 | 0 | Reserved |

## PHASE DETECTOR (PD) REGISTER

**Table 24. Register 0x0B, PD Register (Default 0x0F8061)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 2:0 | R/W | PD_DEL_SEL | 3 | 1 | Sets the PD reset path delay (recommended setting is 001). |
| 4:3 | R/W | Reserved | 2 | 0 | Reserved. Combined separate values shown on 704, using defaults – ok. |
| 5 | R/W | PD_UP_EN | 1 | 1 | Enables the PD up output. |
| 6 | R/W | PD_DN_EN | 1 | 1 | Enables the PD down output. |
| 8:7 | R/W | CSP mode | 2 | 0 | Cycle slip prevention mode. This delay varies by ±10% with temperature and ±12% with process. Extra current (~8mA) is driven into the loop filter when the phase error is larger than the following:<br>0 = disabled.<br>1 = 5.4 ns.<br>2 = 14.4 ns.<br>3 = 24.1 ns.<br>CSP should only be used with comparison frequencies <= 50MHz, otherwise disable. Always confirm loop stability when using CSP. |
| 9 | R/W | Force CP up | 1 | 0 | Forces CP up output to turn on; use for test only. |
| 10 | R/W | Force CP down | 1 | 0 | Forces CP down output to turn on; use for test only. |
| 11 | R/W | Force CP Mid-Rail | 1 | 0 | Forces CP to Mid-Rail; use for test only. |
| 19:12 | R/W | Reserved | 13 | 248d (0xF8) | Reserved. |
| [21:20] | R/W | Divider Pulse Width | 2 | 0 | 0: Shortest…3: Longest |
| [23:22] | R/W | Reserved | 1 | 0 | Reserved. |

## EXACT FREQUENCY MODE REGISTER

**Table 25. Register 0x0C, Exact Frequency Mode Register (Default 0x000000)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 13:0 | R/W | Number of Channels per $f_{PD}$ | 14 | 0 | The comparison frequency divided by the correction rate must be an integer. Frequencies at exactly the correction rate have zero frequency error.<br>0: disabled.<br>1: disabled.<br>2:16383d (0x3FFF). |

## GENERAL-PURPOSE, SPI, AND REFERENCE DIVIDER (GPO_SPI_RDIV) REGISTER

**Table 26. Register 0x0F, GPO_SPI_RDIV Register (Default 0x000001)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 4:0 | R/W | GPO_SELECT | 5 | 1d | The signal selected by this bit is an output to the LD/SDO pin when the LD/SDO pin is enable via Register 0x08[5]<br>0: data from Register 0x0F[5]<br>1: lock detect output<br>2: lock detect trigger<br>3: lock detect window output<br>4: ring oscillator test<br>5: pull-up resistor is ~230 Ω from CSP<br>6: pull-down resistor is ~230 Ω from CSP<br>7: reserved<br>8: reference buffer output<br>9: reference divider output<br>10: VCO divider output<br>11: modulator clock from VCO divider<br>12: auxiliary clock<br>13: auxiliary SPI clock<br>14: auxiliary SPI enable<br>15: auxiliary SPI data output<br>16: PD down<br>17: PD up<br>18: internal clock path (SD3) clock delay<br>19: SD3 core clock<br>20: auto-strobe integer write<br>21: auto-strobe fractional write<br>22: auto-strobe auxiliary SPI<br>23: SPI latch enable<br>24: VCO divider sync reset<br>25: seed load strobe<br>26 to 29: not used<br>30: SPI output buffer enable<br>31: soft reset, $\overline{\text{RST}}$ |
| 5 | R/W | GPO test data | 1 | 0 | 1: GPO test data |
| 6 | R/W | Prevent automux SDO | 1 | 0 | 1: outputs GPO data only<br>0: automuxes between SDO and GPO data |
| 7 | R/W | LDO driver always on | 1 | 0 | 1: LD/SDO pin driver always on<br>0: LD/SDO pin driver only on during SPI read cycle<br>Prevents SPI from disabling SDO. Set to 1 if using HMC SPI mode. |
| 8 | R/W | Disable PFET | 1 | 0 | 0: enable LD/SDO pin high drive<br>1: disable LD/SDO pin high drive |
| 9 | R/W | Disable NFET | 1 | 0 | 0: enable LD/SDO pin low drive<br>1: disable LD/SDO pin low drive |

## VCO TUNE REGISTER

The VCO tune register is a read only register.

**Table 27. Register 0x10, VCO Tune Register (Default 0x000020)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 7:0 | R | VCO switch setting | 8 | 32 | Indicates the VCO switch setting selected by the autocalibration state machine to yield the nearest free running VCO frequency to the desired operating frequency. Not valid when Register 0x10[8] = 1, autocalibration busy. When a manual change is made to the VCO switch settings, this register does not indicate the current VCO switch position. VCO subsystems may not use all the MSBs, in which case the unused bits are don't care bits.<br>0 = highest frequency.<br>1 = second highest frequency.<br>…<br>255 = lowest frequency. |
| 8 | R | Autocalibration busy | 1 | 0 | Busy when the autocalibration state machine is searching for the nearest switch setting to the requested frequency. |

## SUCESSIVE APPROXIMATION REGISTER

The successive approximation register (SAR) is a read only register.

**Table 28. Register 0x11, Successive Approximation Register (Default 0x07FFFF)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 18:0 | R | SAR error magnitude counts | 19 | $2^{19}$ to 1 | SAR error magnitude counts |
| 19 | R | SAR error sign | 1 | 0 | SAR error sign<br>0 = error is positive<br>1 = error is negative |

## GENERAL-PURPOSE 2 REGISTER

The GPO2 register is a read only register.

**Table 29. Register 0x12, GPO2 Register (Default 0x000000)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 0 | R | GPO | 1 | 0 | GPO state |
| 1 | R | Lock detect | 1 | 0 | Lock detect status<br>1 = locked<br>0 = unlocked |

## BUILT-IN SELF TEST (BIST) REGISTER

The BIST register is a read only register.

**Table 30. Register 0x13, BIST Register (Default 0x001259)**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 16:0 | R | Reserved | 17 | 4697d | Reserved |

# VCO SUBSYSTEM REGISTER MAP

The VCO subsystem uses indirect addressing via Register 0x05. Unlike the PLL registers Since the VCO contains 3 registers and all will be accessed via PLL Register 0x05 it is necessary to add the VCO Chip ID (0x000) and VCO Register Address (0x00xx) prior to sending the VCO Data bits shown below. For more detailed information on how to write to the VCO subsystem, see the VCO Serial Port Interface (VSPI) section.

The VCO tuning register is write only.

**Table 31. VCO_REG 0x00, Tuning Register**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 0 | W | CAL | 1 | 0 | VCO tune voltage is redirected to a temperature compensated calibration voltage |
| 8:1 | W | CAPS | 8 | 16 | VCO sub-band selection<br>0000 0000: maximum frequency<br>1111 1111: minimum frequency |

## VCO POWER REGISTER

The VCO power register is a write only register.

**Table 32. VCO_REG 0x01, Enable Register**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 1:0 | W | RFOUT power control | 2 | 0 | Nominal RFOUT power 0: 2dBm, 1: 3 dBm, 2: 4dBm, 3: 5dBm |
| 4:2 | W | VCO bias control | 3 | 0 | 0: Low current mode … 7: High performance mode (need to add table) |
| 6:5 | W | Divider output power | 2 | 0 | 0: -4dBm, 1: 0dBm, 2: 0dBm, 3: dBm (nominal SE power level of PDIVOUT / NDIVOUT |
| 7 | W | Reserved | 1 | 0 | Reserved, program to 0d |
| 8 | W | PD Divider | 1 | 0 | 0: Power down differential output divider, 1: Differential output divider on |

### *Example: Optimizing the Output Power using the VCO Subsystem*

For optimum phase noise and maximum RFOUT power using the subsystem of the ADF5610, set Bits 7 through 13 in VCO_REG 0x01. If the other bits are left unchanged, write 0 0111 1111 into VCO_REG 0x01. The VCO subsystem register is accessed via a write to PLL subsystem Register 0x05 = 0 0111 1111 0001 00 = 0x3F88.

Register 0x05[2:0] = 000b; VCO subsystem ID 0.

Register 0x05[6:3] = 0001b; VCO subsystem register address.

Register 0x05[8:7] = 11b; RFOUT maximum output power, +5dBm nominally.

Register 0x05[11:9] = 111b; VCO bias, high performance mode.

Register 0x05[13:12] = 11b; PLL buffer enable.

Register 0x05[14] = 0b; Reserved.

Register 0x05[15] = 0b; Disable differential output divider (improves RFOUT power level by ~1dBm)

## VCO DIFFERENTIAL OUTPUT DIVIDER REGISTER

This is a write only register. In order to make use of the divider ratio settings, the divider must first be enabled via VCO_REG_01[8] = 1.

**Table 33. VCO_REG 0x02, Output Divider Register**

| Bit | Type | Name | Width | Default | Description |
|---|---|---|---|---|---|
| 2:0 | W | RF divide ratio | 3 | 0 | 0: $f_O$/128<br>1: $f_O$/64<br>2: $f_O$/32<br>3: $f_O$/16<br>4: $f_O$/8<br>5: $f_O$/4<br>6: $f_O$/2<br>7: $f_O$/1 (bypass) |
| 3 | W | VCO EN | 1 | 0 | 0: Enable VCO, 1: Power down VCO |
| 8:4 | W | Reserved | 5 | 0 | Reserved, program 0d |

### *Example: Setting the Differential Output Divider to Divide-by-64 via the VCO Subsystem*

The VCO registers are written in reverse order (highest to lowest). First we will set the divide ratio, then we will enabled the divider, finally we'll select the band.

To write 0 0000 0001 into VCO_REG 0x02 (VCO_ID = 000b) and set the VCO output divider to divide by 64, the following must be written to Register 0x05 = 0 0000 0001 0010 000 = 0x0090.

Register 0x05[2:0] = 000; Subsystem ID 0

Register 0x05[6:3] = 000; VCO Register Address 2d.

Register 0x05[16:7] = 0 0000 0001; divide by 64, maximum output RF gain.

Next, using the same settings that were used for bits [14:0] in the example for VCO_REG_01 we'll enabled the differential output divider by simply change VCO_REG_01[15] = 1 writing 1 0111 1111 into VCO_REG 0x01. The full VCO subsystem write via PLL Register 0x05 = 0 0111 1111  0001 000 = 0xBF88. The individual bitfield settings to achieve this are shown below.

Register 0x05[2:0] = 000b; VCO subsystem ID 0.

Register 0x05[6:3] = 0001b; VCO subsystem register address.

Register 0x05[8:7] = 11b; RFOUT maximum output power, +5dBm nominally.

Register 0x05[11:9] = 111b; VCO bias, high performance mode.

Register 0x05[13:12] = 11b; PLL buffer enable.

Register 0x05[14] = 0b; Reserved.

Register 0x05[15] = 1b; Enable differential output divider (note that RFOUT power level will drop by ~1dBm)

If no VCO band change is required, register writes are complete.

If this is the first write to the synthesizer or if re-writing all of the PLL registers,  a write to REG 0x05 = 0 which allows a subsequent frequency change via autocalibration is required. The last write in the PLL register sequence triggers the frequency update. If an integer value will result at the phase detector input, the last write in the register sequence will be PLL REG 0x03, if it will be a fractional value then it will be PLL REG 0x04.

If the band for the desired RFOUT frequency (prior to division) is already known, this could be written to directly via VCO_REG 0x00 by disabling the temperature controlled VTUNE calibration voltage and manually selecting the band via VCO_REG_0x00.

For example, assume that the desired RFOUT frequency prior to division is 8 GHz and falls in band 205. After writing the above sequences for VCO_REG 0x02 and VCO_REG 0x01 we would write 1 1001 1010 into VCO_REG 0x01. The full VCO subsystem write via PLL Register 0x05 = 1 1001 1010 0000 000 = 0xCD00. The individual bitfield settings to achieve this are shown below.

Register 0x05[2:0] = 000b; VCO subsystem ID 0.

Register 0x05[6:3] = 0000b; VCO subsystem register address.

Register 0x05[7] = 0b; disable autocalibration.

Register 0x05[15:8] = 1100 101b (205d); band 205 = band 77 of the lower VCO core.

# EVALUATION PRINTED CIRCUIT BOARD (PCB)

The circuit board used in the application uses RF circuit design techniques. Signal lines have 50 Ω impedance, whereas the package ground leads and exposed pad are connected directly to the ground plane. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation board details are available from Analog Devices upon request.

## EVALUATION KIT CONTENTS

The evaluation kit contains one EV1ADF5610LP6G evaluation PCB, a USB interface board, a six-foot USB Type A male to USB Type B female cable, a CD ROM that contains the user manual, evaluation PCB schematic, evaluation software, and Analog Devices PLL design software.

# OUTLINE DIMENSIONS

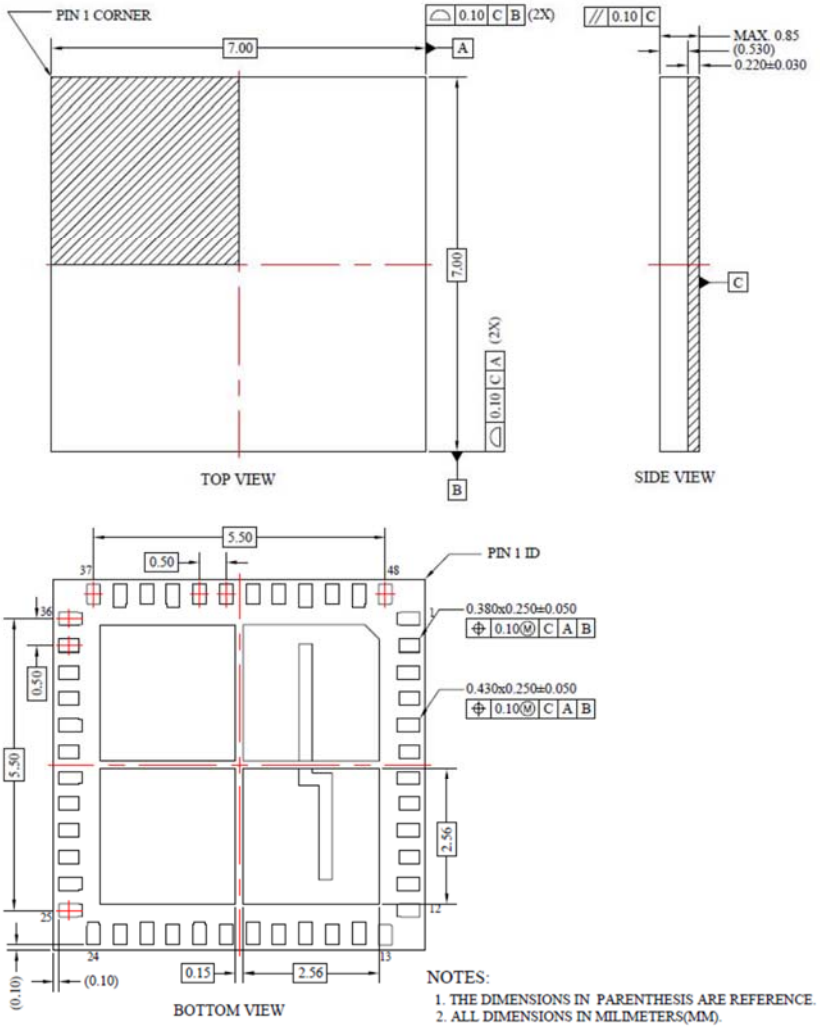



*Figure 33. 48-Lead Land Grid Array Package (LGA)*
*7 mm x 7mm Body*
*Dimensions shown in millimeters.*

**Note:** Exposed Pad (EP) is a solid plane of Cu except for the slot which minimizes substrate warpage. During solder attach it's acceptable for solder to bridge across the opening in the slot. The solder mask opening creates a "window pane" effect to minimize voiding.

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