RZ MPU INTRODUCTION FOR ON-LINE SEMINAR

(RZ/G, RZ/A & RZ/V)

VERSION: 1.0

PREPARED BY: ANGUS CHAN

SECTION 4
BIZ DEVELOPMENT DEPT.
EPMP / EPBD / SOC
RENESAS ELECTRONICS CHINA LTD.

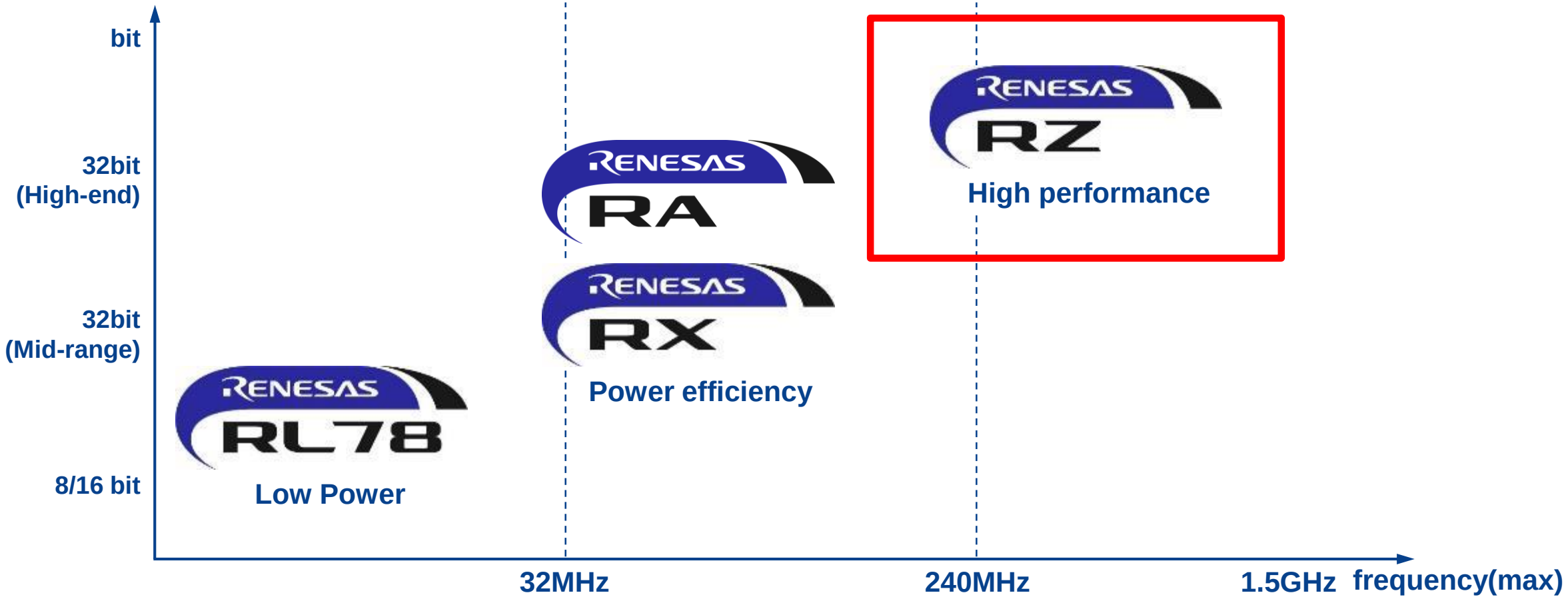
MAR-2020

AGENDA

- Renesas MPU Series Overview
- Today's Target Product Offering
- MPU Series Detailed Explanation
  - RZ/G Series
  - RZ/A Series
  - RZ/V Series

Renesas Microcontroller Expansion

■ Progressive expansion with RL78 family, RX family, RA family, RZ family as a new family



RZ Family

Demonstrate maximum performance for Industrial network & HMI

Human machine interface

RZ/G Series

Multimedia /3D Graphics + Linux

RZ/A & RZ/V Series

2D Graphics + RTOS

RENESAS RZ

Industrial Network & Real-time control

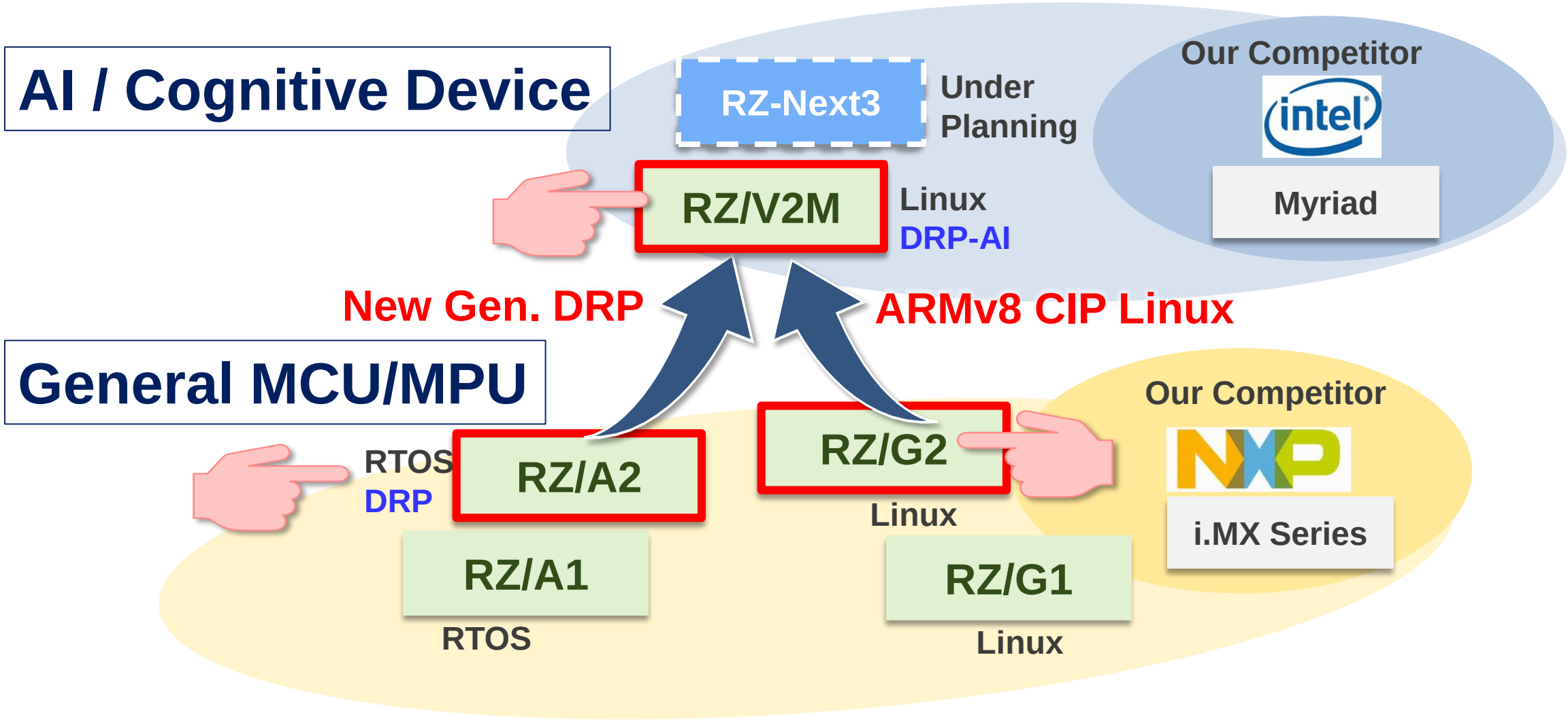
RZ/N Series

Multi-protocol Industrial Ethernet +
5ports GMAC with Switch & Redundancy

RZ/T Series

Real-time control+
Multi-protocol Industrial Ethernet

Today's Target Product Offering

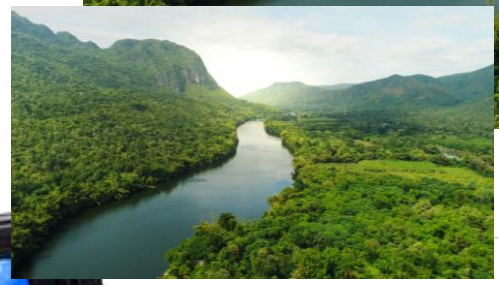


RZ/G SERIES

FOR REFERENCE:

GUI RESOLUTIONS BY RENESAS DEVICE

3840 x 2160



1920 x 1080

1280 x 800

800 x 600

4K UHD — **RZ/G2**

HD 1080 — **RZ/G1**

WXGA — **RZ/A1**

SVGA — **Synergy S5 & S7**

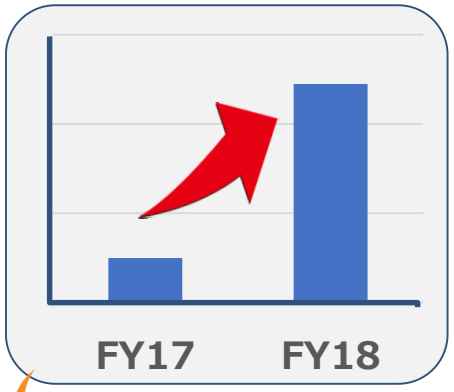
Synergy S1 & S3

Segment Displays — **RL78**

RZ/G New Release for Market Expansion with 64bit Linux

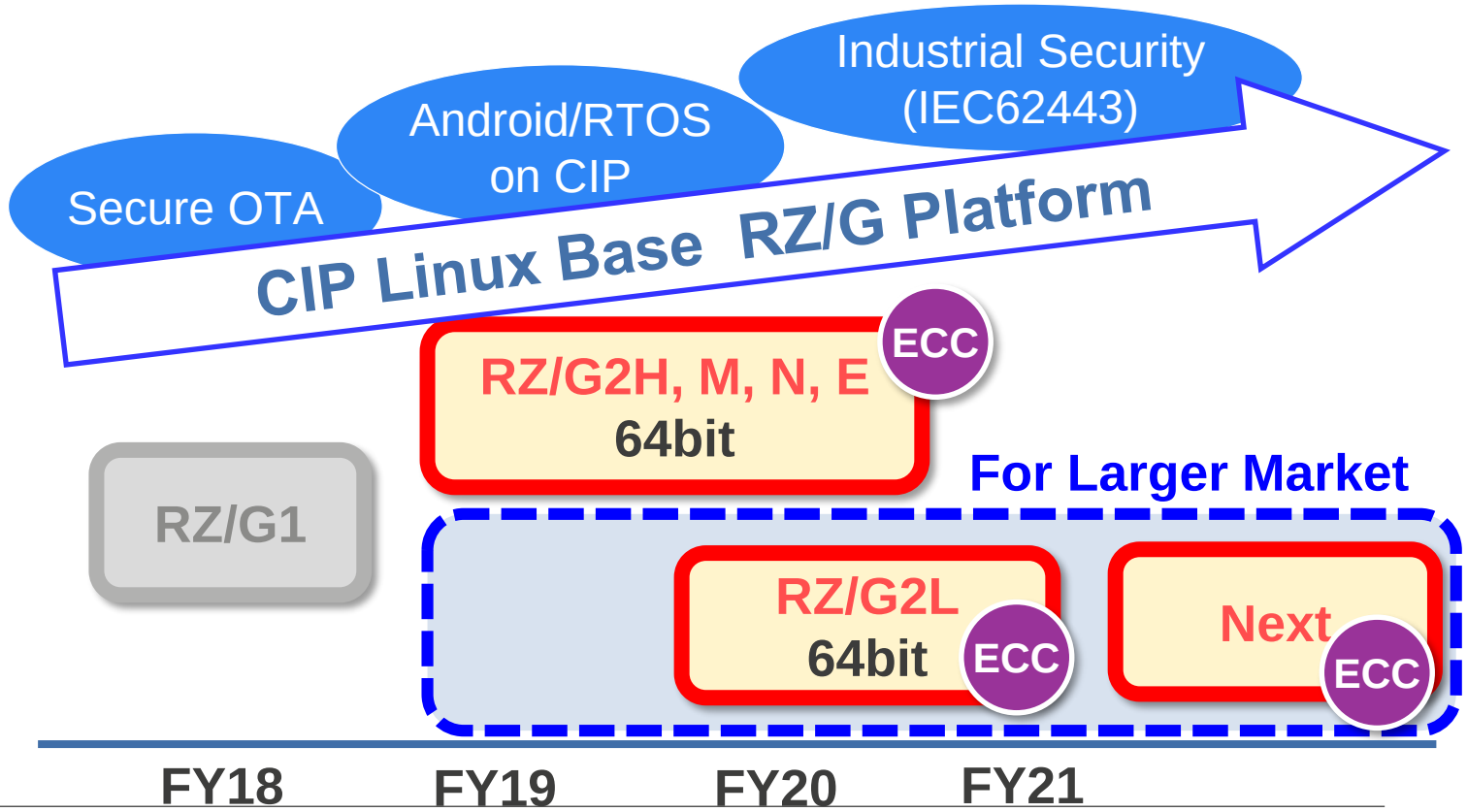
CIP Linux for Long-term Maintenance

CIP related biz. D-in 5x



CIVIL INFRASTRUCTURE PLATFORM

RZ/G Solution Roadmap



RZ/G Linux Platform with

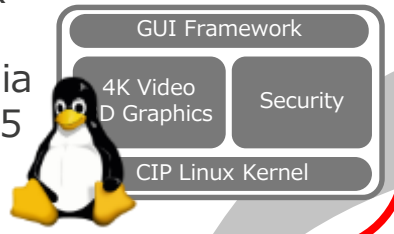
Industry-grade CIP Linux reduces risk and cost of ownership

One package software framework

✓ **Verified Linux Package**

- CIP Linux
- Security
- Multimedia
- Qt/HTML5

CIVIL INFRASTRUCTURE PLATFORM

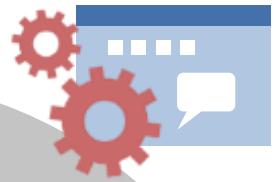


RZ/G Processor

RENESAS RZ

✓ RZ/G1 Series
✓ RZ/G2 Series

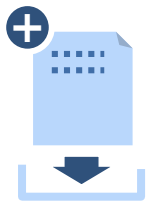
Development environment



✓ Linux customization tool
✓ Validation / analysis tool
✓ Smart Configurator

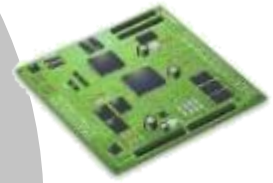
Solution Software Add-on

✓ Unique Partner Middleware



RZ/G Linux Platform

Evaluation Board



✓ Partner Board
- 96Board
- iWave

Verified Linux Package (VLP)

Customers can use verified S/W including middleware necessary for HMI, Application development can start from a stable operating environment

Verified

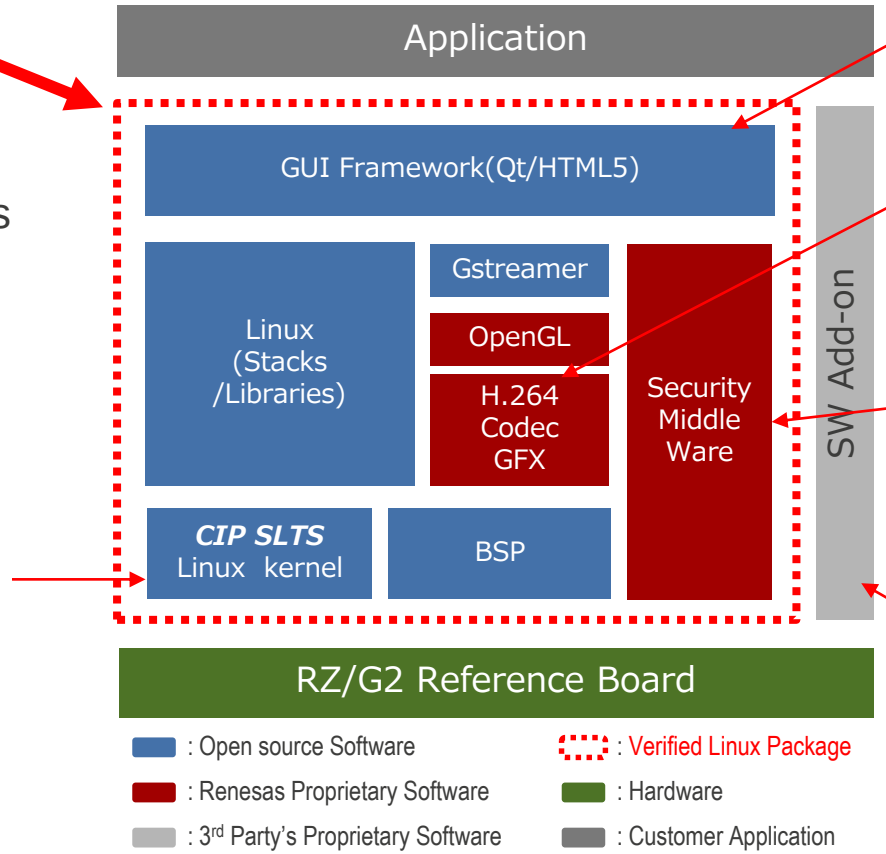
- Renesas carries out verification
- Software development process management of CMMI level 3
- Provide evidence of verification results

CIVIL INFRASTRUCTURE PLATFORM

CIP Super Long-Term support Kernel

- Civil Infrastructure Platform project
- 10+ years super long term support
  Reliability/Security/Real-time

(cf. LTSI kernel: 2-3years support)



GUI Framework

- Qt application framework
- HTML5 application framework

Multimedia

- H.264 Codec
- H.265 Decoder
- 3D graphics

Secure Middle Ware

- Encrypted kernel boot
- Security communication
- Secure storage

Renesas sample applications

3rd party SW add-on

RZ/G Key Advantage

① For Industrial: Super long-term Linux (CIP) and HW Reliability (ECC)

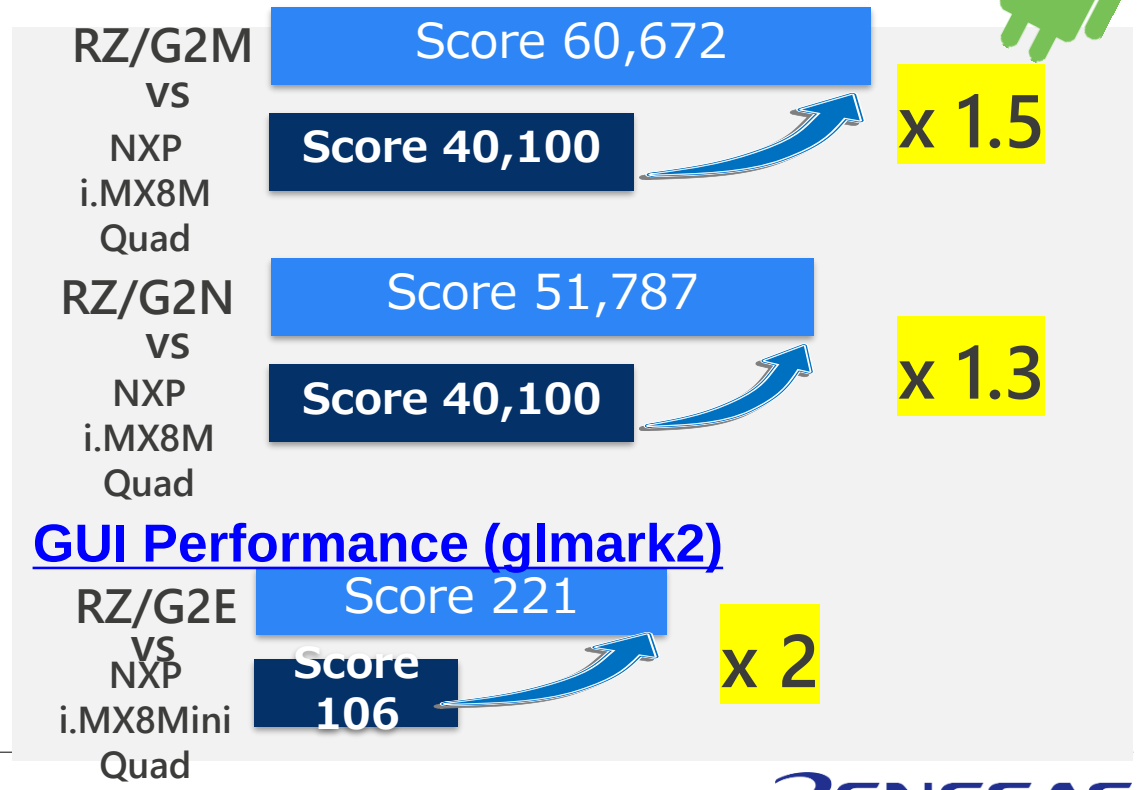
② For HMI System: Higher system performance than NXP i.MX8.

① Strength for Industrial Application

Company		Renesas		Competitor Nxx	
Device Lineup	High	RZ/G2H	ECC	×	-
	Mid-H	RZ/G2M	ECC	i.MX8 QMax	-
	Mid-L	RZ/G2N, E	ECC	i.MX8X	ECC
				8M, Mini	-
	Entry	RZ/G2L	ECC	×	-
SW	Linux Kernel	"Industrial Grade" Linux CIP 10+ years maintenance		2 years maintenance	

② Strength for HMI System

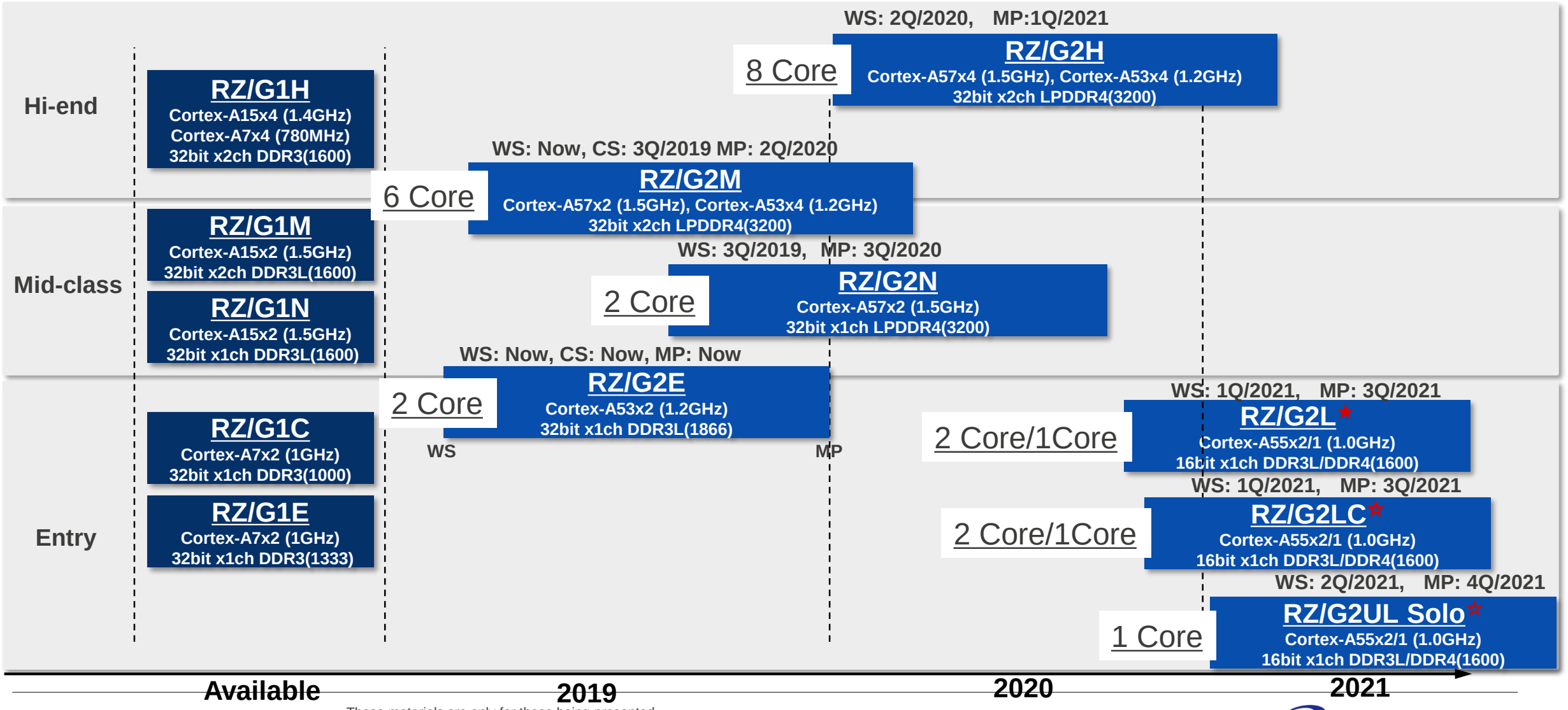
Android Performance (Antutu v6.3.7)



GUI Performance (glmark2)

RZ/G2 Series Roadmap

★ Under development
☆ Under Planning



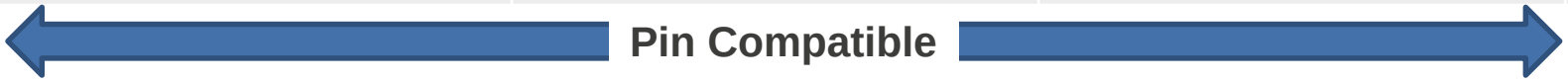
RZ/G1 Specifications

	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1C	RZ/G1E
CPU	4x Cortex-A15@1.4GHz 4x Cortex-A7@780MHz (25kDMIPS)	2x Cortex-A15@1.5GHz (10.5kDMIPS)	2x Cortex-A15@1.5GHz (10.5kDMIPS)	2x Cortex-A7@1.0GHz (3.8kDMIPS)	2x Cortex-A7@1.0GHz (3.8kDMIPS)
DRAM I/F	32bit x2ch DDR3-1600	32bit x2ch DDR3L-1600	32bit x1ch DDR3L-1600	32bit x1ch DDR3-1000	32bit x1ch DDR3-1333
Video in	Video In x4ch (Digital)	Video In x3ch (Digital)	Video In x3ch (Digital)	2ch selectable Video In x2(Digital) /CVBS In x1	Video In x2ch (Digital)
Video Codec	Up to Full-HD x 2ch	Up to Full-HD x 1ch	Up to Full-HD x 1ch	Up to Full-HD x 1ch	Up to Full-HD x 1ch
3D GFX	PowerVR G6400@520MHz	PowerVR SGX544MP2@520MHz	PowerVR SGX544MP2@312MHz	PowerVR SGX531@260MHz	PowerVR SGX540@260MHz
Display out	RGB888 x1ch LVDS x2ch	RGB888 x1ch LVDS x1ch	RGB888 x1ch LVDS x1ch	2ch selectable RGB888 x2/ LVDS x1/CVBS out x1	RGB888 x2ch
USB2.0	USB2.0 x2ch	USB2.0 x2ch	USB2.0 x2ch	USB2.0 x2ch	USB2.0 x2ch
Ether	1Gb Ethernet 10-100 Ethernet	1Gb Ethernet or 10-100 Ethernet	1Gb Ethernet or 10-100 Ethernet	1Gb Ethernet or 10-100 Ethernet	1Gb Ethernet 10-100 Ethernet
USB3.0/PCIe/SATA	PCIe /SATA x1ch USB3.0/SATA x1ch	PCIe /SATA x1ch USB3.0/SATA x1ch	PCIe /SATA /USB3.0 x1ch	No	No
Package	831pin 27mm x 27mm 0.8mm ball pitch	831pin 27mm x 27mm 0.8mm ball pitch	831pin 27mm x 27mm 0.8mm ball pitch	501pin 21mm x 21mm 0.8mm ball pitch	501pin 21mm x 21mm 0.8mm ball pitch

RZ/G2 Specifications

★ Under development

	RZ/G2H★	RZ/G2M★	RZ/G2N★	RZ/G2E★
	Wide-Range Scalable & Pin compatible Products (37.6k~14.3k DMIPS)			Economical
CPU	4x Cortex-A57@1.5GHz 4x Cortex-A53@1.2GHz (37.6kDMIPS) Parity/ECC	2x Cortex-A57@1.5GHz 4x Cortex-A53@1.2GHz (25.3kDMIPS) Parity/ECC	2x Cortex-A57@1.5GHz (14.3kDMIPS) Parity/ECC	2x Cortex-A53@1.2GHz (7.5kDMIPS) Parity/ECC
DRAM I/F	32bit x2ch LPDDR4(3200) w/ECC	32bit x2ch LPDDR4(3200) w/ECC	32bit x1ch LPDDR4(3200) w/ECC	32bit x1ch DDR3L(1866) w/ECC
Video in	2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8input image can be captured	2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8input image can be captured	2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8input image can be captured	1xMIPI-CSI2, 1xDigital(RGB/YCbCr) up to 2input image can be captured
Video Codec	Support up to 4k resolutions Decoding : H.265, Encoding and Decoding : H.264	Support up to 4k resolutions Decoding : H.265, Encoding and Decoding : H.264	Support up to 4k resolutions Decoding : H.265, Encoding and Decoding : H.264	Support up to FHD resolutions Decoding : H.265, Encoding and Decoding : H.264
3D GFX	PowerVR GX6650@600MHz	PowerVR GX6250@600MHz	PowerVR GE7800@600MHz	PowerVR GE8300@600MHz
Display out	1xHDMI, 1xLVDS, 1x Digital RGB	1xHDMI, 1xLVDS, 1x Digital RGB	1xHDMI, 1xLVDS, 1x Digital RGB	2xLVDS or 1xLVDS, 1x Digital RGB
USB	USB2.0 x 2ch (1H, 1H/F/OTG) USB3.0/2.0 x1ch (DRD)	USB2.0 x 2ch (1H, 1H/F/OTG) USB3.0/2.0 x 1ch (DRD)	USB2.0 x 2ch (1H, 1H/F/OTG) USB3.0/2.0 x 1ch (DRD)	USB2.0 x 1ch (H/F) USB3.0/2.0 x1ch (DRD)
Gbit Ether	1ch	1ch	1ch	1ch
PCIe	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	2ch (Rev2.0 1Lane)	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	1ch(Rev2.0 1Lane)
SATA	1ch(Pin Shared)	No	1ch（Pin Shared）	No
Package	1022pin FCBGA, 29mm x 29mm 0.8mm ball pitch	1022pin FCBGA, 29mm x 29mm 0.8mm ball pitch	1022pin FCBGA, 29mm x 29mm 0.8mm ball pitch	552pin FCBGA, 21mm x 21mm 0.8mm ball pitch



RZ/G2 Key Solutions and Benefits

RZ/G delivers advantages by combining hardware and software

High Performance

64-bit ARMv8A plus powerful graphics engine and 4K UHD video engine offers higher performance per dollar than competing embedded 64-bit MPUs

- Cortex-A53 CPU and Cortex-A57
- Up to 8 cores
- Power VR 3D Graphics
- H.265 Playback, H.264 Recoding/Playback

High Reliability

Built-in Error Correction Code (ECC) essential for high-reliability mission critical systems. Reduces and or eliminates soft errors

- ECC for internal L1 and L2 cache
- ECC for external DDR memory interfaces
- ECC built into all RZ/G2 products

Super Long Term Support (SLTS)

Civil Infrastructure Platform (CIP) offers 10+ years support for Linux kernel

- Security maintenance for over 10 years
- Real-Time Patches for CIP kernel

RZ/G Verified Linux Package (VLP)

Reduce development cost and time with Renesas verified software for RZ/G MPUs

- VLP tested and maintained by Renesas
- VLP Includes CIP Linux kernel
- Development can start immediately

Function Extension Points

From RZ/G1 to RZ/G2

	RZ/G1 Group	RZ/G2 Group
CPU	32bit ARMv7-A Cortex-A15 Cortex-A7	64bit ARMv8-A Cortex-A57 Cortex-A53
DRAM I/F	DDR3/DDR3L	DDR3L/LPDDR4 (ECC)
Video	FHD resolutions H.264/AVC	4K resolutions H.265 Decoder H.264/AVC
3D GFX	PowerVR	PowerVR Latest Version
Display out	LVDS, RGB888	HDMI,LVDS,RGB888
Video in	Digital (RGB/YCbCr) Max 4	MIPI-CSI2,Digital (RGB/YCbCr) Max 8
Security	Cryptographic processing engine (AES、DES、Hash function、RSA)	Cryptographic processing engine (AES、DES、Hash function、RSA) TrustZoon
Other peripheral functions	USB3.0, SATA, PCI-e, Giga Bit Ether	USB3.0, SATA, PCI-e, Giga Bit Ether

Adopted as RZ/G2 board CIP standard

Improve industrial safety and reliability

Supports 4K display

MIPI support for image input

Improved security

RZ/G2 Series Applications

Industrial Automation

- Industrial HMI, Panel PC
- CNC, PLC
- Testing Equipment

Building Automation

- HVAC Controller
- Security Panel, Digital Signage
- Gate Control
- Surveillance (Elevator, etc.)

Camera Application Other

- Surveillance Camera, Multi-camera
- Intercom, IP Phone, Conference
- Audio Equalizer, Karaoke
- Patient Monitor, Surveillance robotics

RZ/A SERIES

Target Application of RZ/A Series

Line up of RZ/A Series

*1 There are freq. limitation
*2 Can be used simultaneously
*3 Option
*4 For industry, consumer

Item	RZ/A1H, RZ/A1M	RZ/A1LU	RZ/A1L	RZ/A1LC	RZ/A2M
CPU/Frequency	Cortex-A9/400MHz				Cortex-A9/528MHz
On-chip RAM	5MB／10MB	3MB		2MB	4MB
Flash ROM	NOR, Serial(DDR*1), NAND	NOR, Serial(DDR)	NOR, Serial(SDR)		NOR, Serial(DDR), NAND, HyperFlash
RAM I/F	SDRAM				SDRAM, HyperRAM
Graphics Acc.	2D(OpenVG)	No			2D
LCD out	VDC5(2ch)	VDC5(1ch)			VDC6(1ch)
Camera I/F	Digital(Parallel) Analog(composite)	Digital (Parallel)			Digital (Parallel/serial:MIPI)
JPEG Codec Unit	Yes		No		Yes
Ethernet	10/100base Ether, x 1, EthenetAVB x1		10/100base Ether x 1		10/100base Ether x2*2, (IEEE1588)
Connectivity	USB2.0 x 2 (FS/HS) SD x 2				USB2.0 x 2(FS/HS/OTG) SD x 2(UHS-I)
Security	Secure Boot *3				Secure Boot *3 Crypto engine *3
Package	256QFP, 324BGA 256BGA*4	176QFP, 208QFP, 176BGA*4	176QFP, 208QFP, 176BGA*4	176BGA*4	324BGA*4, 272BGA*4, 256BGA*4, 176BGA*4
Status	MP	MP	MP	MP	Under developing

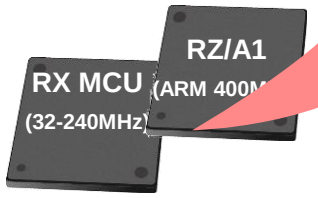
Device Roadmap

- e-AI Class-3 devices have powerful HW AI Engine(DRP-AI).
- Enhance cognitive solution furthermore with these strong AI accelerator devices.

CY2017 CY2019 CY2019 CY2020 CY2021 CY2022

[Device roadmap]

e-AI Class-1



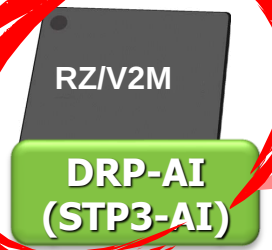
x10

WS : Done
MP : 2019/3Q

e-AI Class-2

x10

e-AI Class-3



x10

e-AI Class-4

[Solution roadmap]

2D Barcode Scanner
18/3Q Release

IRIS Scanner
19/1Q Release

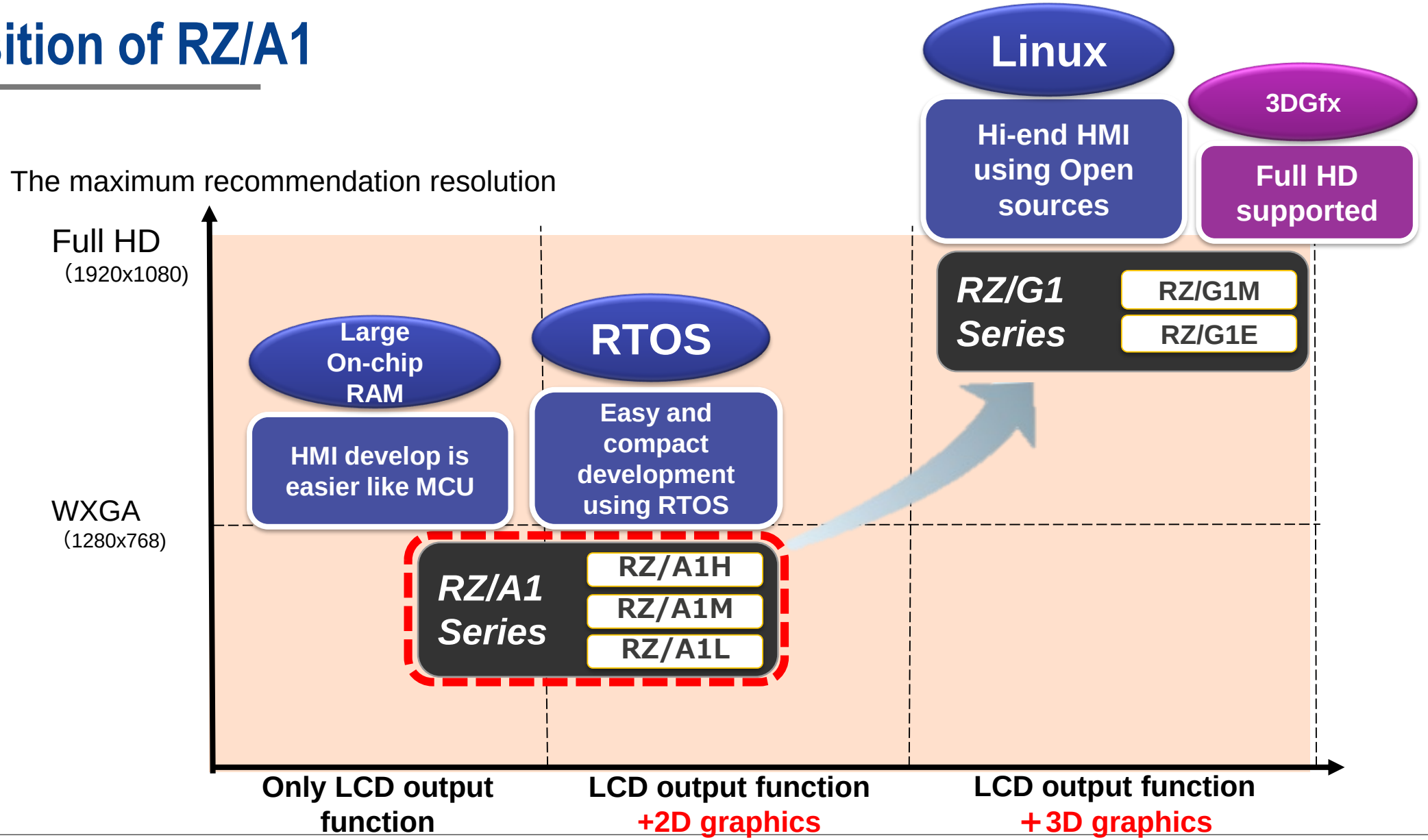
Face Recognition
& Authentication

California
123-456

Automatic License
Plate Recognition

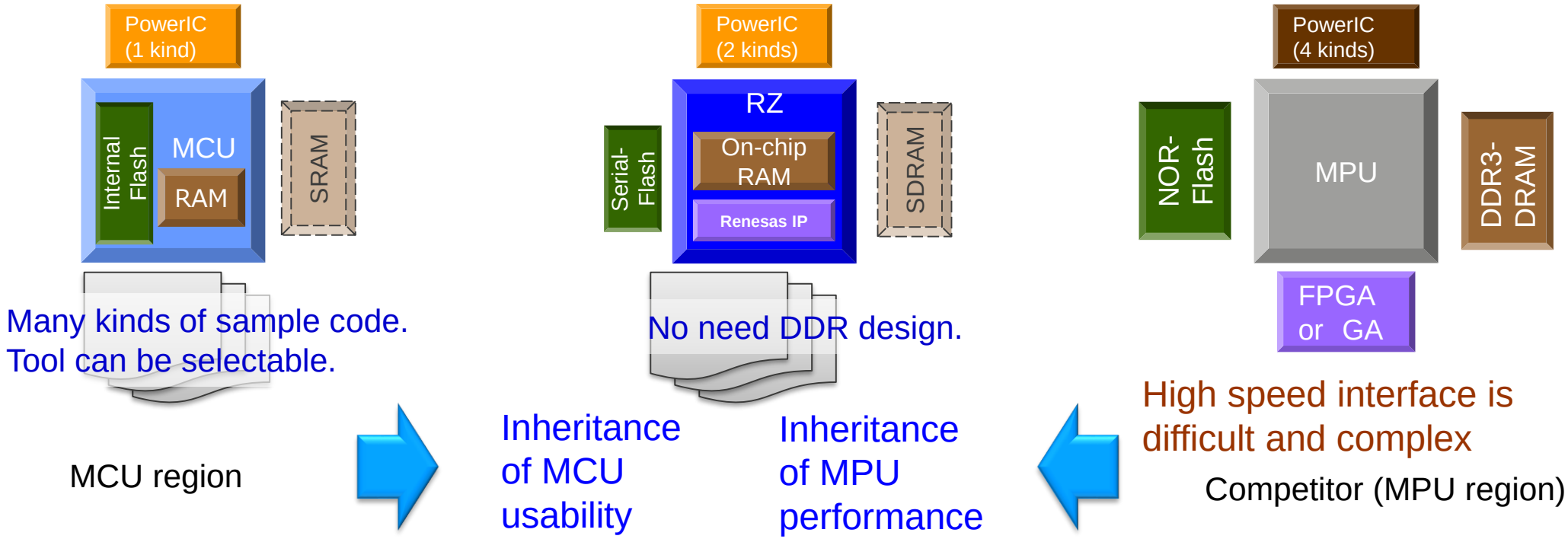
To be continued
(Colored area is under planning)

Position of RZ/A1



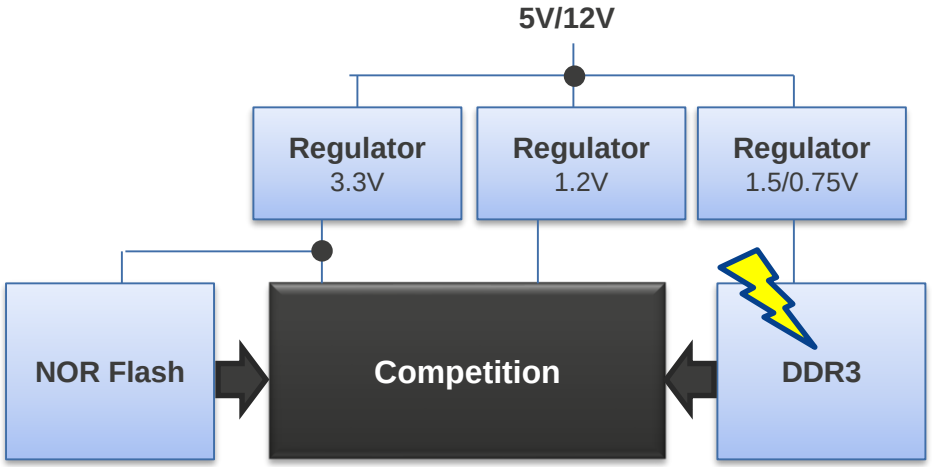
Concept of RZ/A1

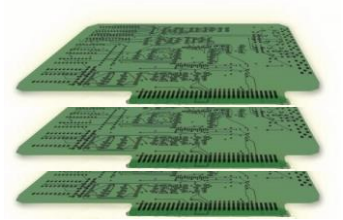
- You can get the MPU performance and MCU concept at the same time!
  - No need external memory: On-chip RAM does not design high speed interface. The problem that DRAM supply issue is gone
  - Rich peripherals: RZ/A1 prepared rich peripherals using SH and RX peripherals



The Benefit On-chip RAM Solution

The concept of traditional MPU

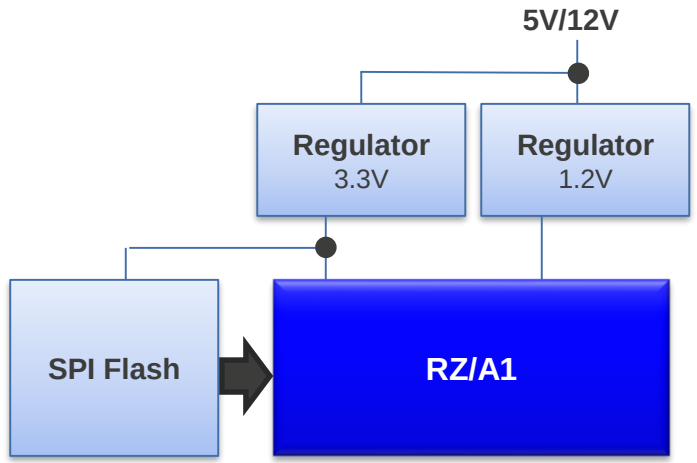


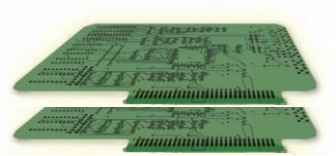


6 PCB layers for 1.2V, 3.3V, 1.5V, 0.75V(DDR3)

- Cost is up
- Power consumption is up
- Mounting area is up
- Noise is up
- Launch time is up
- Complex design
- Quality correspondence is difficult
- Availability is difficult
- Long term procurement is difficult

The Concept of RZ/A1

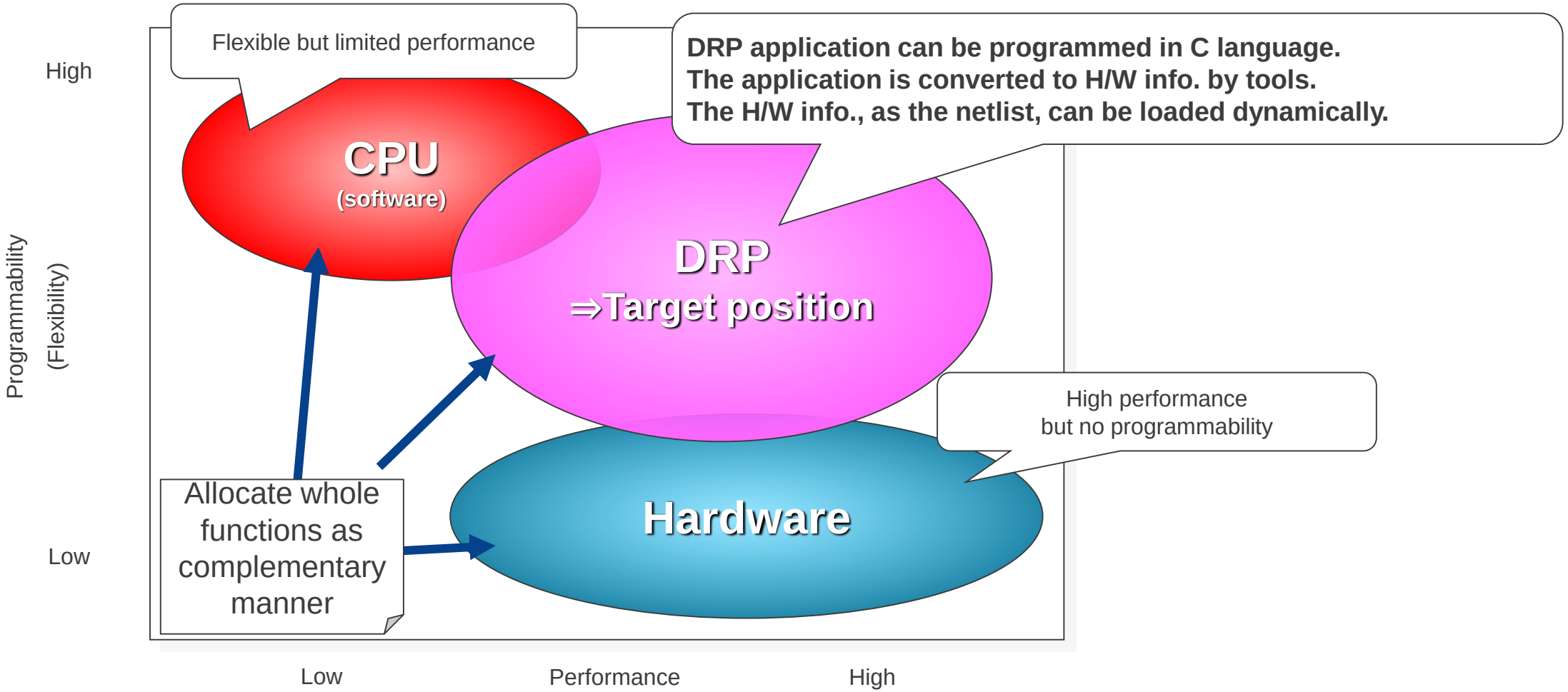




4 PCB layers for 1.2V, 3.3V

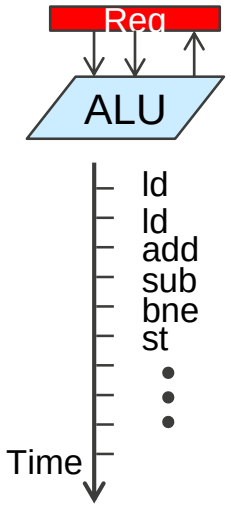
RZ/A2M (by DRP Technology)

PERFORMANCE AND FLEXIBILITY



HOW DRP WORKS?

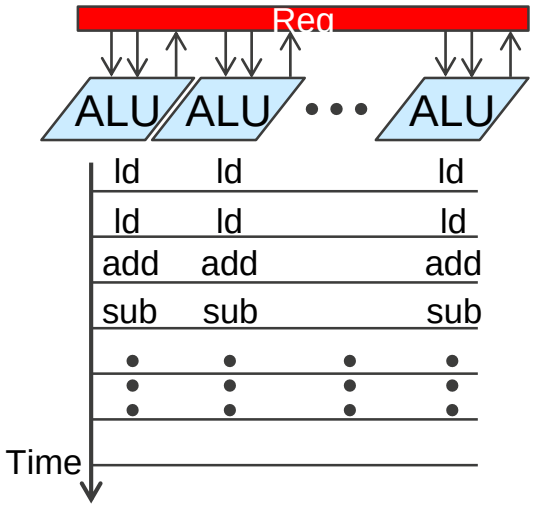
CPU



Process 1 to a few operations in a cycle

优 Flexibility
劣 Performance
优 Area efficiency

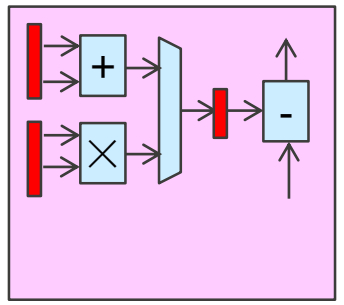
GPU (SIMD)



Process 10-100 same operations in a cycle

优 Flexibility
劣 Performance
优 Area efficiency

FPGA

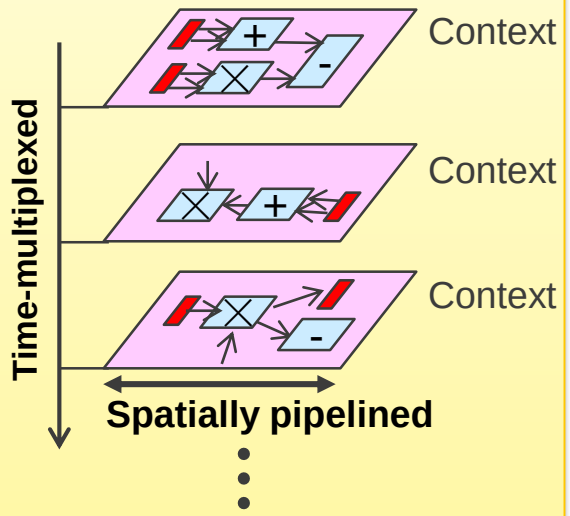


Pipelined processing

Spatially expand various operations into LUT

劣 Flexibility
优 Performance
劣 Area efficiency

DRP



Process spatially and temporally expanded operations

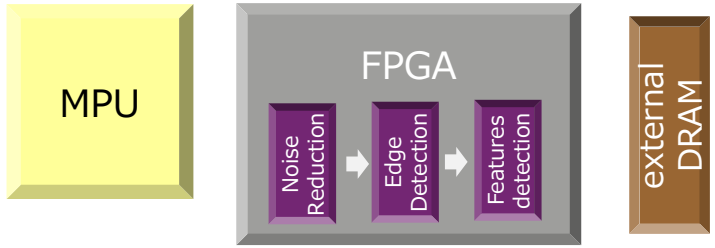
良 Flexibility
良 Performance
良 Area efficiency

FLEXIBILITY BY DYNAMIC LOADING

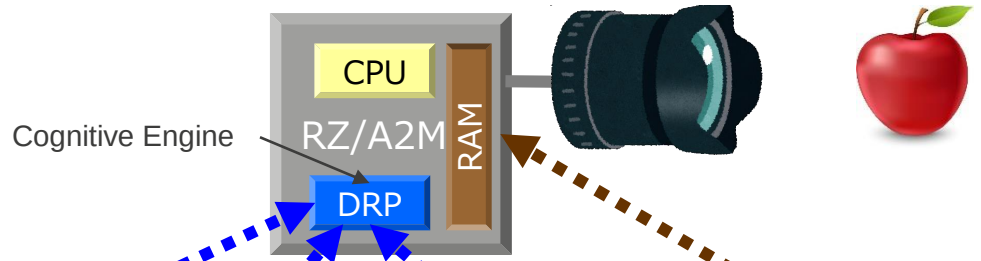
By taking advantage of the short switching time less than 1 ms, the circuit is dynamically replaced every processing step required for object recognition.

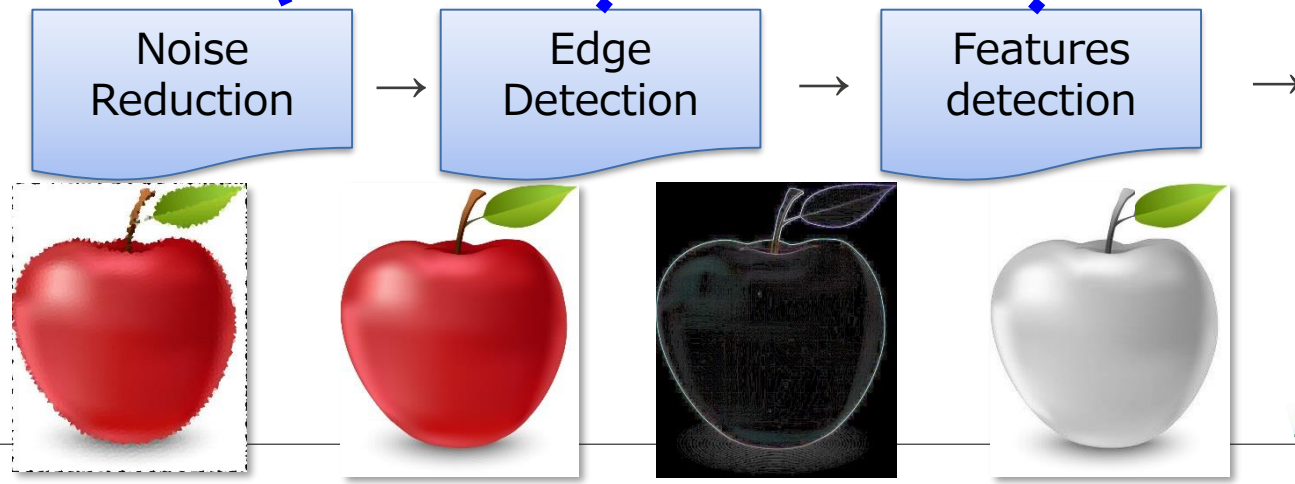
→ Provide flexibility and efficiency that can not be provided by fixed HW of FPGA.

Conventional example when image processing is implemented by FPGA
(It is necessary to implement all required processing circuits)



Example of image processing by DRP

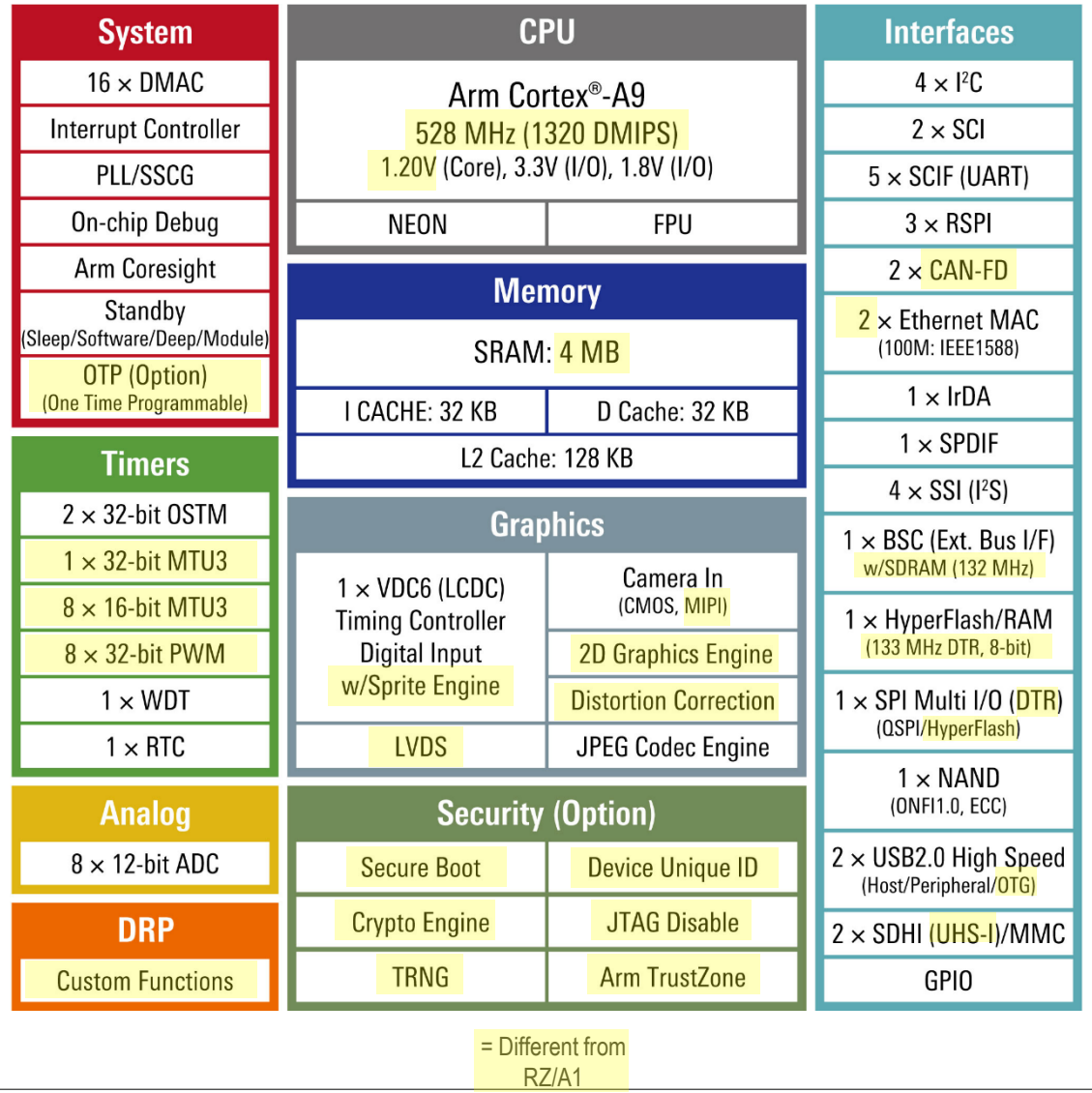




RZ/A2M

FIRST RZ WITH DRP

- **e-AI Class-2**
  - DRP Multipurpose Accelerator
- **Large 4MB SRAM**
  - High-speed access & Low BOM Cost
- **High performance**
  - Cortex-A9 528MHz with NEON DSP
  - 2D Graphics accelerator & Sprite Engine
  - Lens-distortion correction
  - JPEG Hardware codec
- **Security**
  - Arm TrustZone
  - Trusted Secure IP (TSIP)
  - Hardware crypto acceleration
  - Key management and storage
  - Access management
- **Packages**
  - 324pin BGA: 19mm/0.8mm pitch
  - 272pin BGA : 17mm/0.8mm pitch
  - 256pin BGA: 11mm/0.5mm pitch
  - 225pin BGA: 8mm/0.5mm pitch (Under planning)
  - 176pin BGA: 13mm/0.8mm pitch



RZ/A2M TARGET APPLICATIONS

Broad Applications

GUI Displays

Factory Automation Displays

Intercoms

Home Appliances

Voice Recognition

Home Appliances

Smart Devices

Communication Robots

DRP-Enabled Applications

Image Recognition

Home Appliances

Facial Recognition

Barcode Scanners

Biometrics

Communication Robots

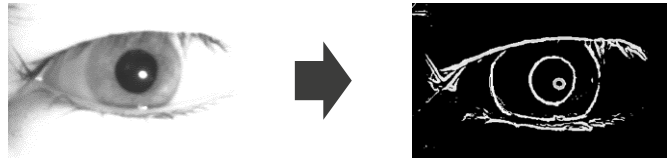
RZ/A2M DRP LIBRARIES

Library for Camera Image Processing

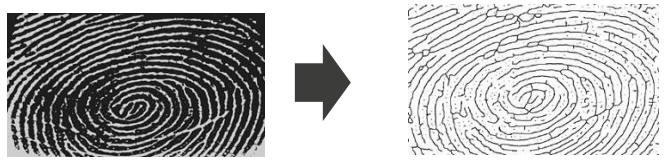
- A library for **processing** image data from a MIPI-based input **in real time**
- Functions such as color transformation, noise reduction, and image treatment are included.
- Each library can be **dynamically loaded** onto the DRP

Library for Image Recognition

- A library which contains the required functions for image recognition, such as feature detection and filter processing
- Pre-processing for 2D barcode, iris recognition, fingerprint recognition, etc. can be accelerated
- **Improves the processing speed of the overall system**, at an **even lower rate of power consumption**.



Canny Edge detection



Thinning

DRP LIBRARY PERFORMANCE

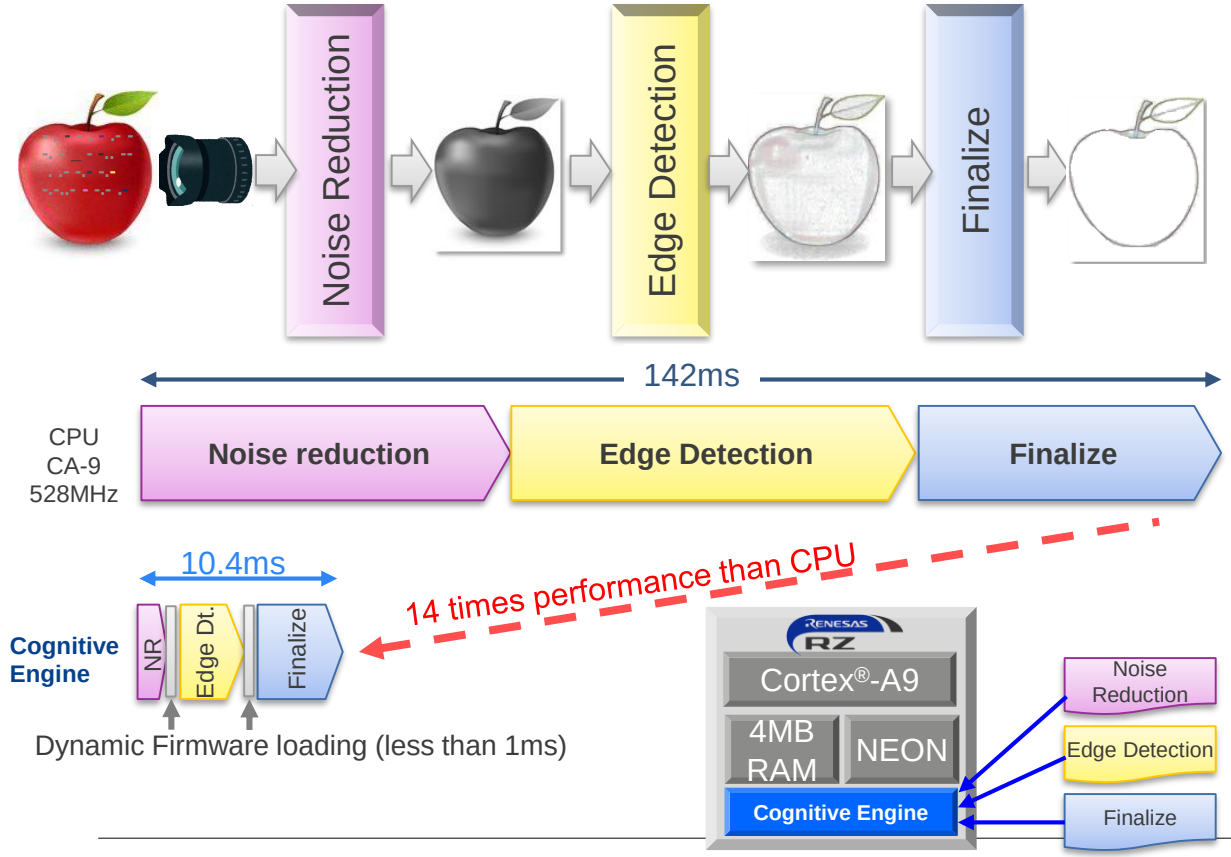
Image size : 640x480 VGA
Image color : Grayscale 8BPP
CPU : RZ/A2M Cortex®-A9@528MHz
RAM : RZ/A2M internal RAM

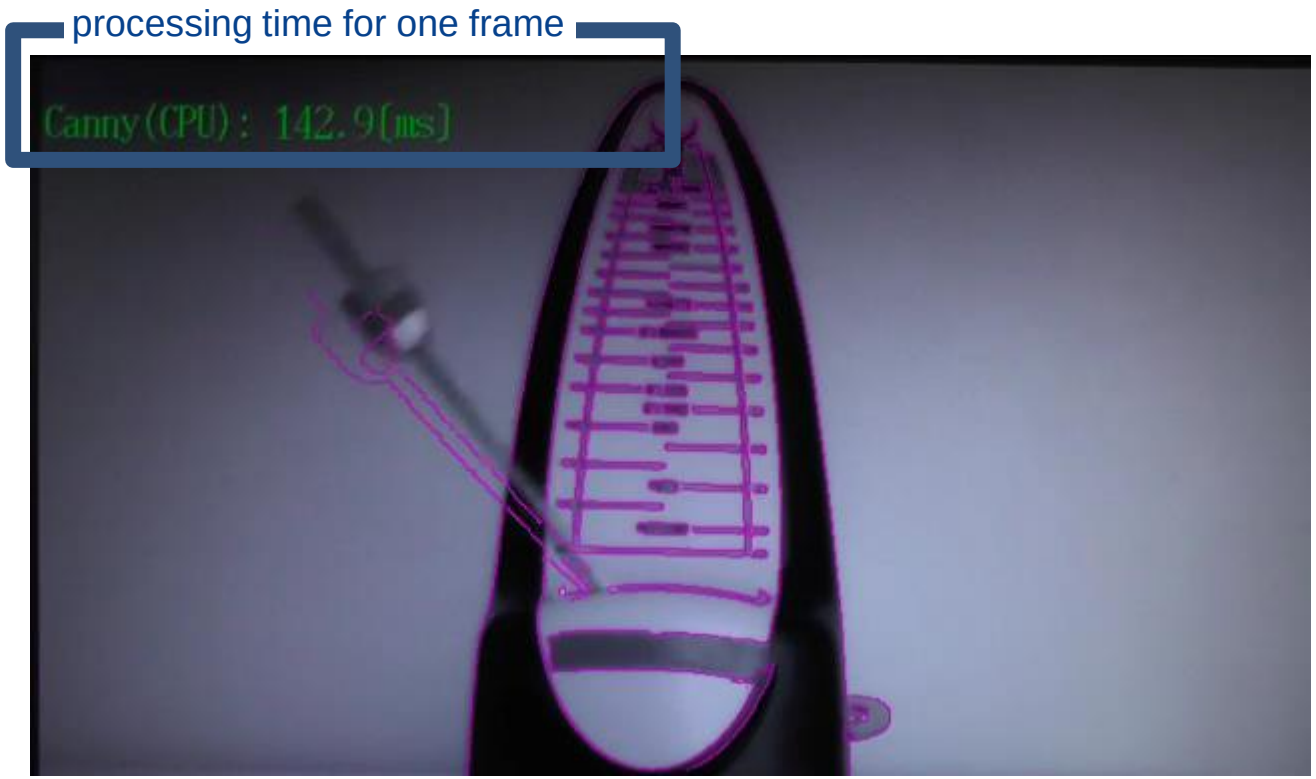
Category	Function	Tiles	Processing performance [ms]			Note
			DRP	CPU	vs CPU	
Image processing	Simple ISP(Bayer to Color)	6	10.87	-	-	
		3	22.22	-	-	
	Simple ISP(Bayer to Grayscale)	6	6.25	-	-	
		3	13.70	-	-	
Color conversion	Bayer to Grayscale	1	0.85	15.3	x 18.0	6 Parallel Processing
	RGB to Grayscale	1	0.61	5.9	x 9.7	6 Parallel Processing
	Binarization(Fixed)	1	0.18	2.3	x 12.8	6 Parallel Processing
	Binarization(Adaptive)	3	1.69	10.1	x 6.0	
Image filtering	Median filter	1	0.85	76.1	x 89.5	6 Parallel Processing
	Gaussian filter	1	0.85	14.4	x 16.9	6 Parallel Processing
	Unsharp masking	2	1.67	34.1	x 20.4	3 Parallel Processing
	Gamma correction	1	0.23	3.8	x 16.5	6 Parallel Processing
Geometric transformation	Cropping	1	0.06	0.2	x 3.3	6 Parallel Processing
	Resize Bilinear Fixed	4	2.24	2.7	x 1.2	
	Resize Bilinear	6	1.29	3.1	x 2.4	
	Resize Nearest	6	0.33	0.6	x 1.8	

Note: Product is still in development, and performance data is subject to change

BENEFIT (1) DYNAMIC LOADING (DEMO MOVIE)

DRP can execute 'Canny' edge detection ten times faster than CPU.
The application contains three independent process.
DRP can switch and execute these process in 10ms using 'Dynamic Loading' capability.





Projector Only

BENEFIT (2) ~ENERGY EFFICIENCY~

■ DRP achieve less than 1/20 energy of CPU for image processing

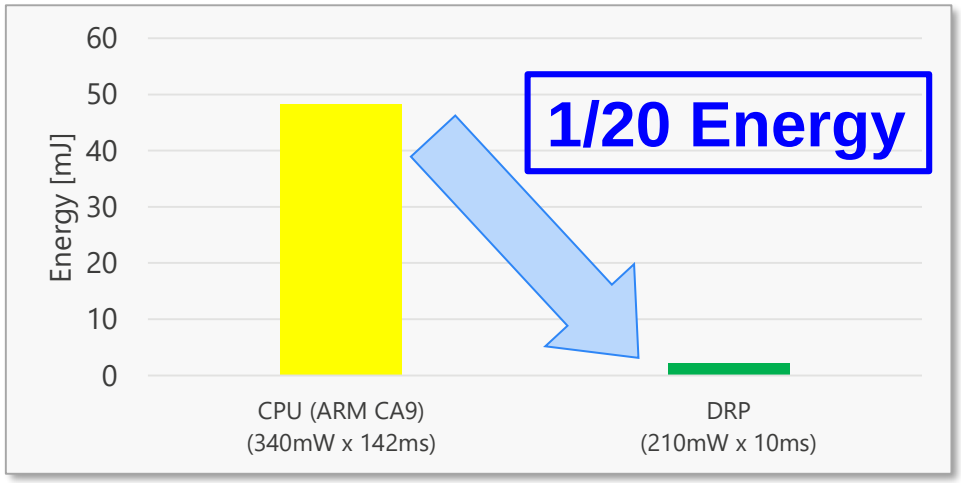
- **We measure power consumption using the RZ/A2M board.**

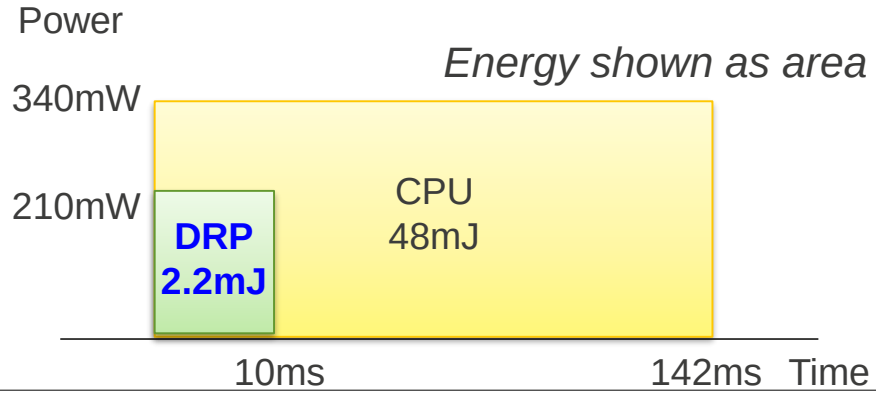
		Operation Frequency	Power Consumption	Execution time	Energy
CPU	Cortex-A9	528MHz	340mW	142 ms (average)	**48 mJ**
DRP	(Class-2) 288 PEs x 64 states	0-66MHz (variable)	210mW	10.4ms (fixed)	**2.2 mJ**

(Condition : typical; room temp. Vdd=1.2V)

Evaluation board

RZ/A2M board





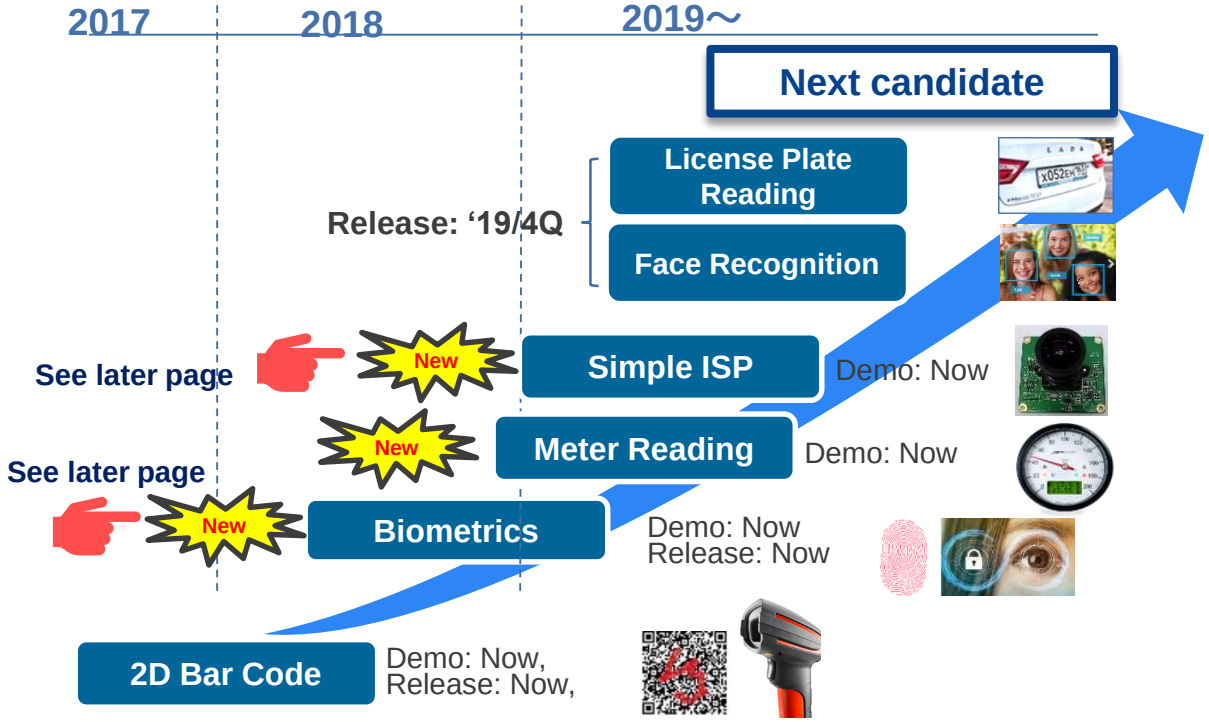
Energy Efficiency Comparison (in Canny Edge Detection per one frame)

BIG IDEAS FOR EVERY SPACE RENESAS

INCREASING DRP SOLUTIONS OF RZ/A2M

- Will release more solutions and expand the lineup (1 development / 3 months)
- Please input your request for the next solutions

Plan of DRP Solutions



Realized high speed & low power by flexible DRP solution

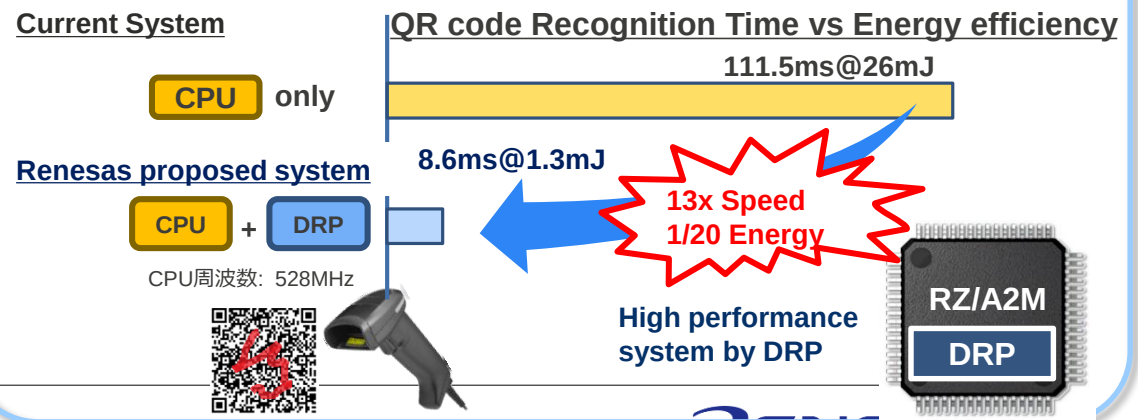
Support Information

・Device	: WS Available (MP: 2019/3Q)
・HW Manual	: Available
・Evaluation Board	: Available
・RZ/A2M Software Package	: Available (Including DRP Library)
・Sales/Promotion Manual	: Available
・WEB Contents	: Available

https://www.renesas.com/jp/ja/products/microcontrollers-microprocessors/rz/rza/rza2m.html

Target Device : RZ/A2M

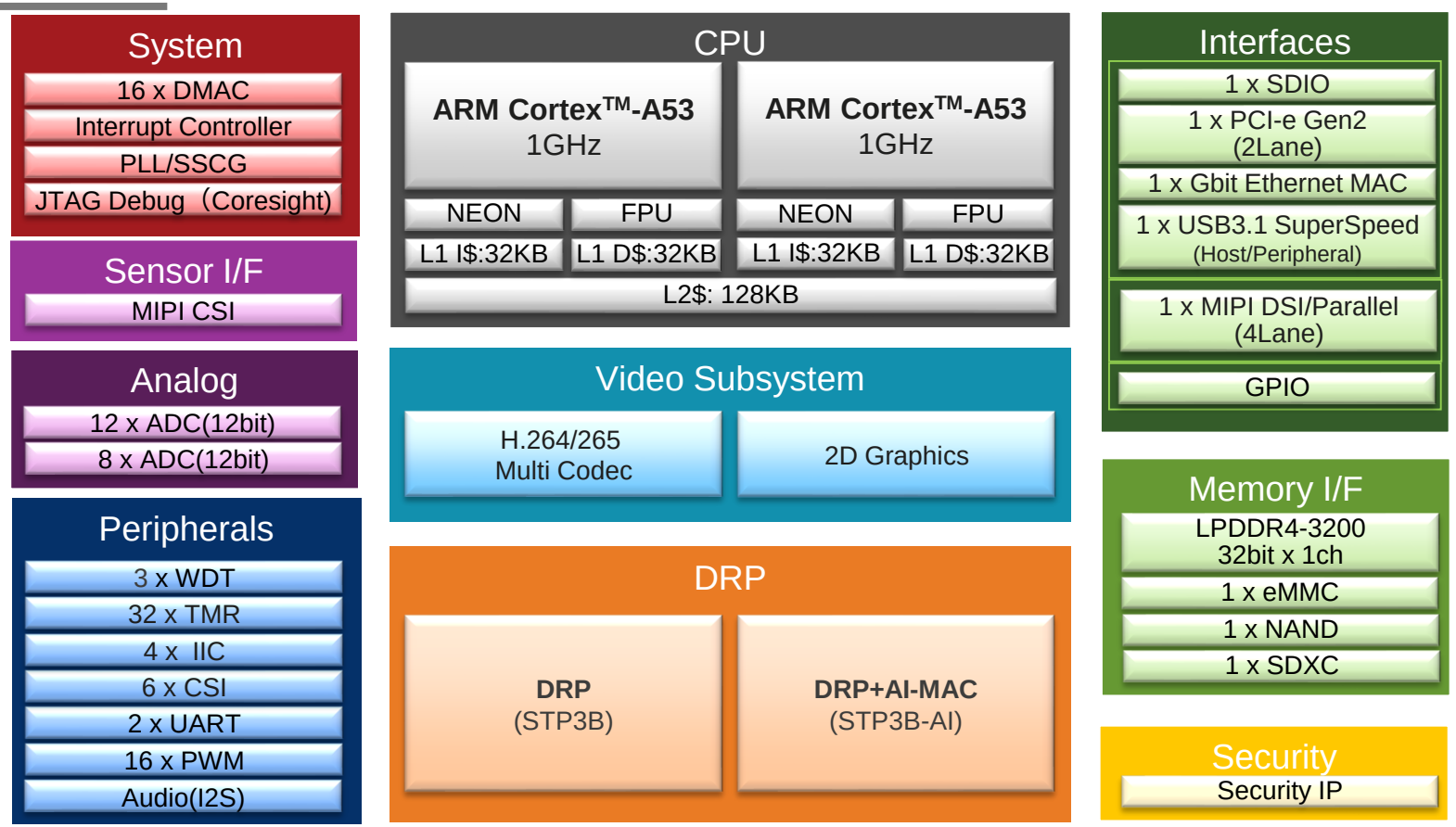
Example : 2D Bar Code Solution



RZ/V SERIES

RZ/V2M LSI SPEC

Under development



Schedule

- Device： ✓ WS：Apr ’20. ✓ MP：Dec ’20 ✓ Manual: Sep ’19(α)
- Development Environment： ✓Linux BSP: Apr ‘20(α) Sep ’20(β)
  ✓e-AI Translator : Jun ’19(α) Sep’19(β)

Power supply：0.8V(Core), 3.3V/1.8V/1.2V/1.1V(I/O)
Package: 841pin FCBGA □ 15mm/0.5mm pitch

※Information on this material is subject to change without notice.

TARGET APPLICATIONS

- AI function/Algorithm might co-work with existing various applications.

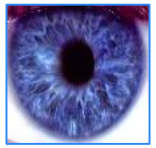
Target Applications

DRP Usage

Image Processing


Barcode


Finger Print


Iris


Face


Object

A,1,あ
Character

Data Processing


Sound


Ultrasonic/TOF


Heat

Application

Code Detection


Scanner


E POS

ID/Access Control


ATM


Office/Building

Inventory Control


Factory/Warehouse

Number Detection


Parking

Guide/Communication Object Detection


CE Robot


Robot

Projector Only

DEMONSTRATION (object recognition by TinyYOLO neural network)

Intel Myriad 2 (SHAVE x12, 600MHz, TinyYOLO/FP16)

Inference Time : 225ms

Framerate : 2.8～3.5 fps

Class-3 DRP-AI Test-chip (FP16 MAC x1024, 400MHz, TinyYOLO/FP16)

Judgement threshold

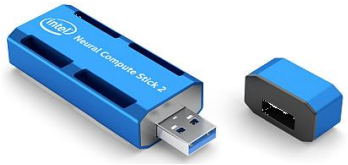
AI processing time of DRP-AI

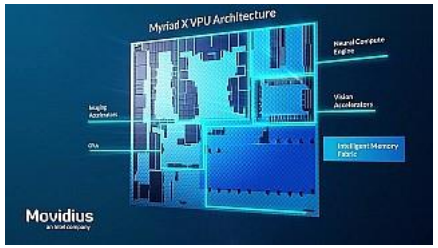
Post processing time of CPU

frame rate

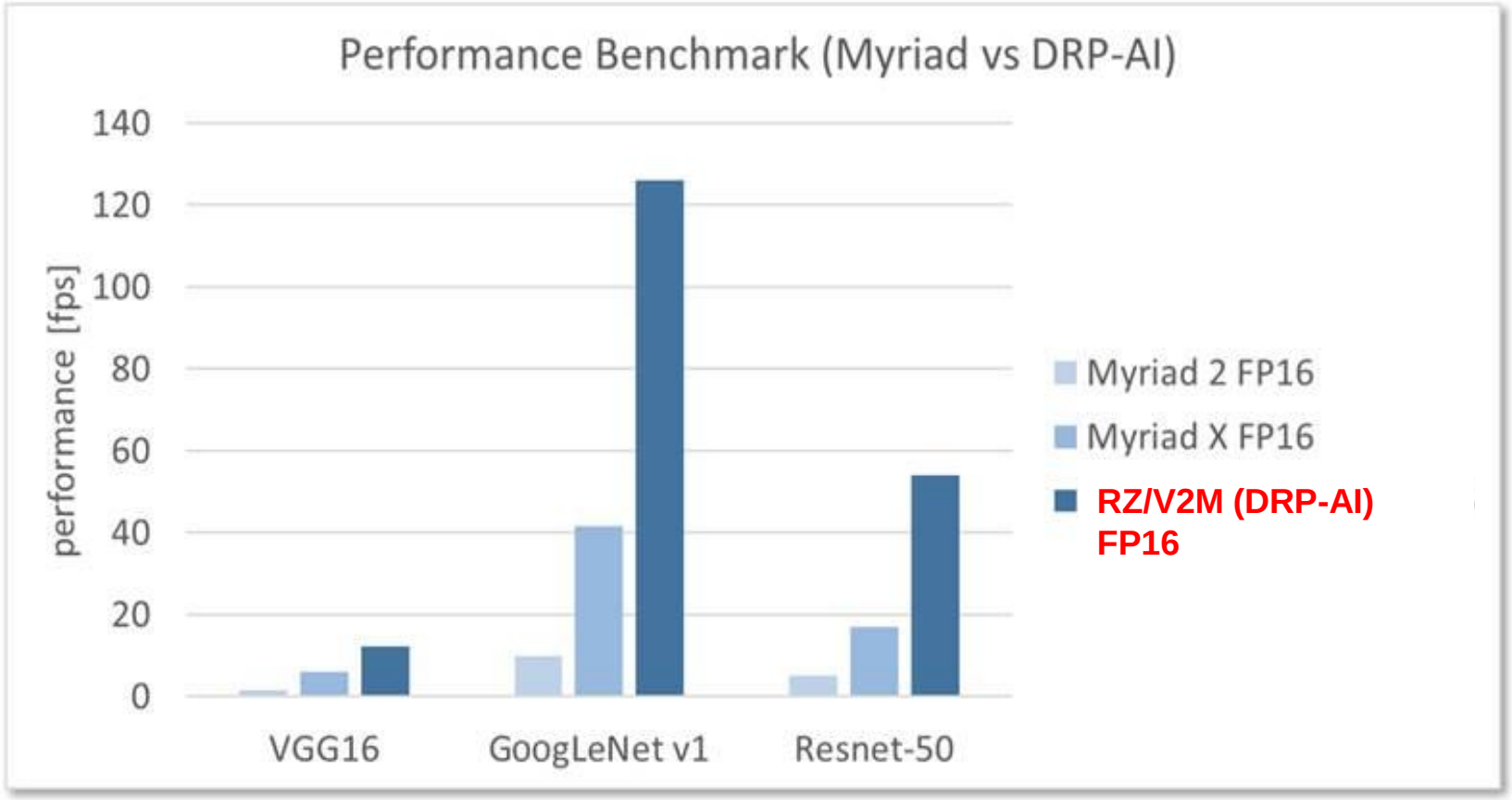
BENCHMARK

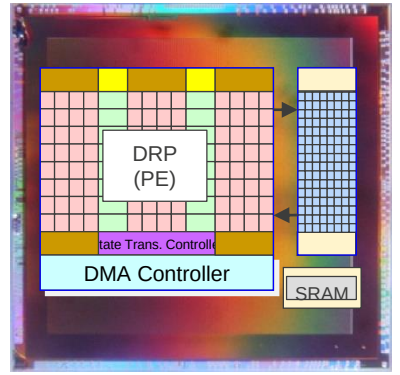
Achieved 3 times performance compared with competitor's AI accelerator





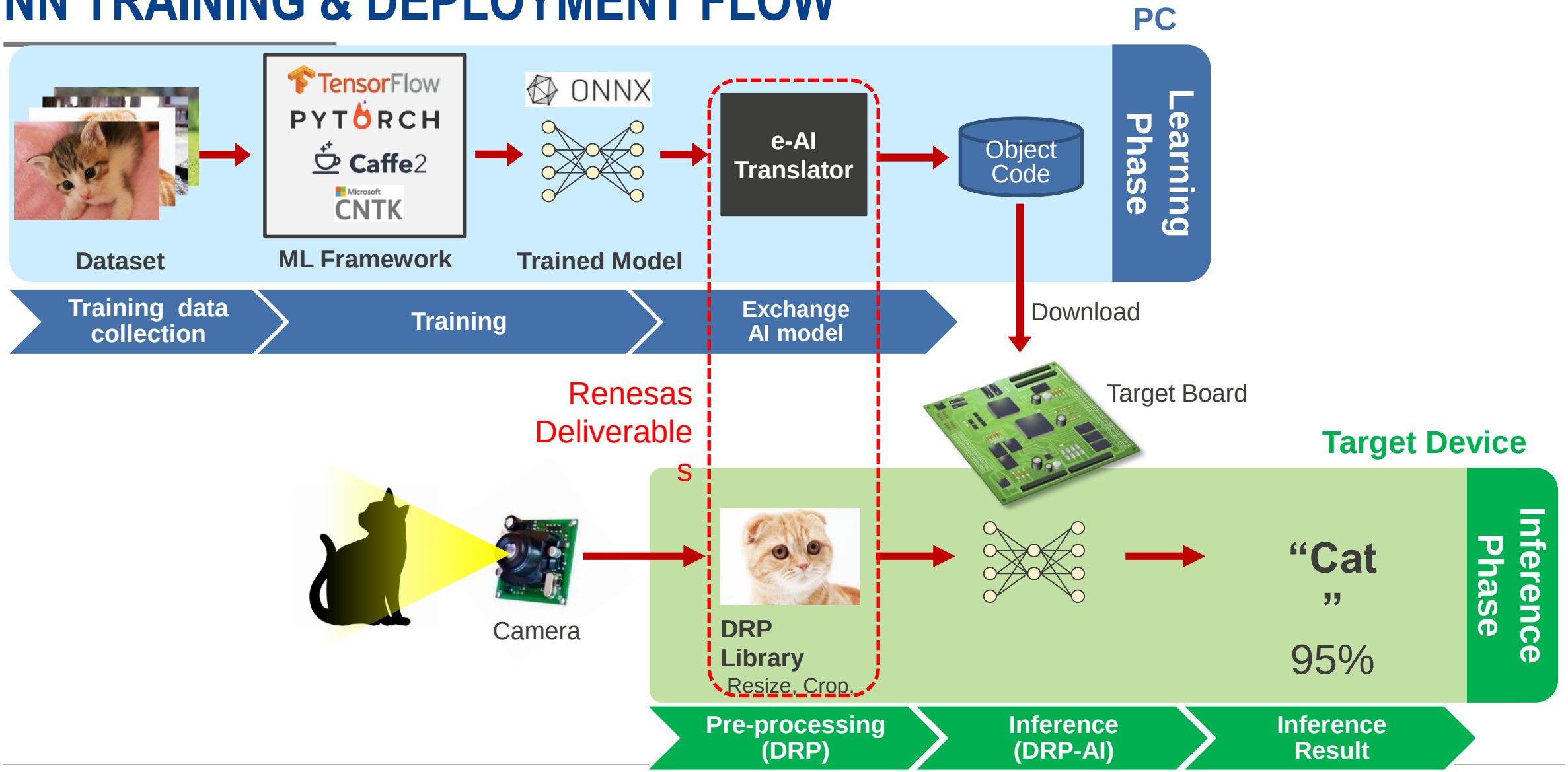
SHAVE(128-bit VLIW) x16
700MHz





FP16 MAC x576@633MHz
16-bit PE x96@333MHz(max)

NN TRAINING & DEPLOYMENT FLOW



RZ/V2M : COMING SOON

- **Sample release product 2Q/’20**
  Mar/’19 : Promotion started using POC, 4Q/’20: MPAI evaluable tool release

	Schedule
POC	Mar./’19
e-AI Tools*	4Q/’19
WS	2Q/’20
MP	4Q/’20

* e-AI translator for DRP, Simulator

Expected Performance

vs nVIDIA Jetson

1/2 ~ 1/3 Low Power

vs Intel Core i5

100x Performance

vs Intel Myriad-X

3x Performance

The first product for DRP-AI

Renesas.com